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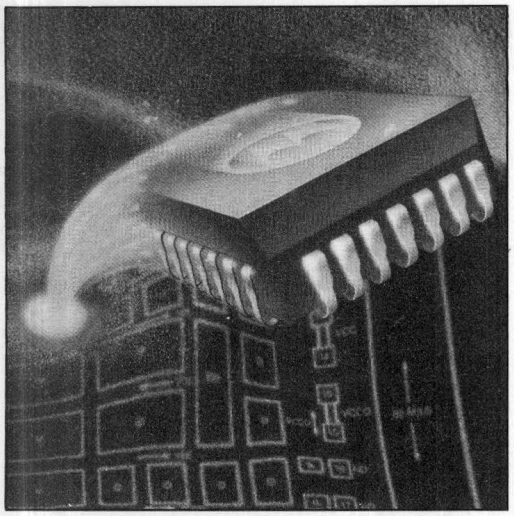
MOTOROLA

ECLinPS DATA



This databook contains device specifications for Motorola's ECLinPS advanced ECL logic family.

ECLinPS (ECL in picoseconds) was developed in response to the need for an even higher performance ECL family of standard logic functions, particularly in the Computer, Automated Test, Instrumentation and Communications industries. Family general features as well as specific functions were developed in close consultation with ECL systems design engineers.

ECLinPS offers the user a single gate delay of 500 ps max., including package delay, and a flip-flop toggle frequency of 1100 MHz.

ECLinPS is compatible with two different ECL standards. Each function is available with either MECL 10KH compatibility (MC10Exxx series) or 100K compatibility (MC100Exxx series).

ECLinPS is offered in the 28-lead plastic leaded chip carrier (PLCC), a J-lead surface mount IC package. This package was selected for high performance, reduced parasitics and good thermal handling in a low cost, standard package, and reflects an industry trend towards surface mount assembly.

Suggested References:

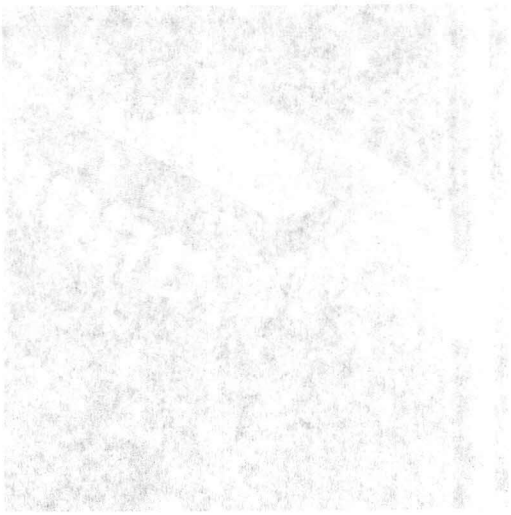
The user is referred to the following for general information on the MECL and 100K ECL families:

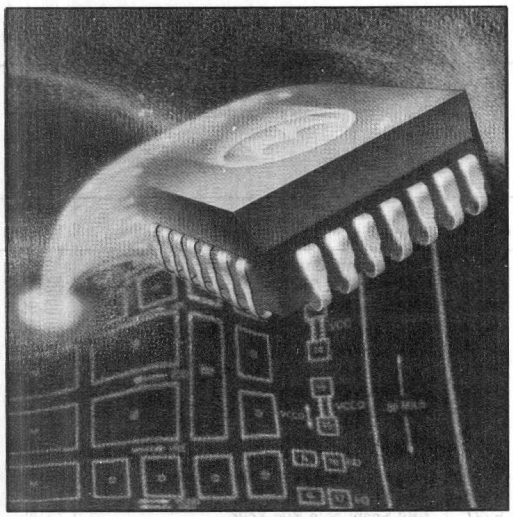
Motorola MECL Device Data Book, Motorola Inc., 1987. Stock code DL122/D.

F100K ECL Data Book, Fairchild Camera and Instrument Corp.

Motorola MECL System Design Handbook, second edition. Motorola Inc., 1983. Stock code HB205R1/D.

Signetics ECL 10K/100K Data Manual.





Numeric Index

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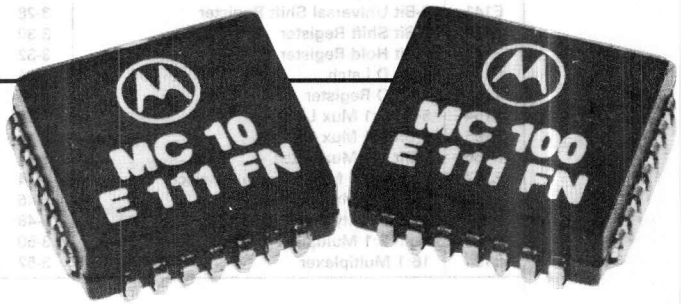

This section lists ECLinPS family functions in numerical order.

MC10E series devices are compatible with the MECL 10KH family. MC100E series are compatible with 100K ECL.

ECLinPS Numeric Index

Numeric Index

MC10/ MC100	Function	Page	MC10/ MC100	Function	Page
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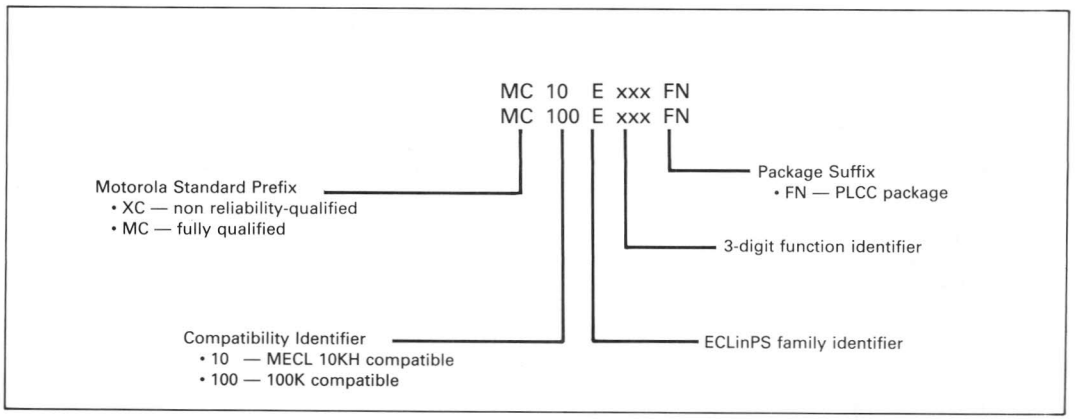
*10E version only

Nomenclature



Selection Guide

Gates

Quad 4-Input OR/NOR	E101
Quint 2-Input AND/NAND	E104
Quint 2-Input XOR/XNOR	E107
Quad 2-Input AND/NAND, Differential	E404

Buffers

9-Bit Buffer	E122
1:9 Differential Clock Driver	E111
Quad Driver with Enable	E112
3-Bit Scannable Driver	E212

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6-Bit D, Diff. Data & CLK Inputs	E451
9-Bit Hold Register	E143
3-Bit D, Edge Triggered Set & Reset	E431
5-Bit Diff. D Reg.	E452

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3-Bit 4:1 Multiplexer	E171
2-Bit 8:1 Multiplexer	E163
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Mux-Latches

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9-Bit Hold Register	E143
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Parity Generator/Comparator

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Line Receivers

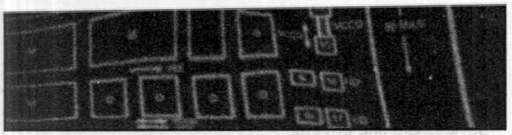
Quint Differential Line Receiver	E116
1:9 Differential Clock Driver	E111
6-Bit D Reg., Diff. Data & CLK Inputs	E451
Quint High Freq. Differential Line Receiver	E416
5-Bit Diff. D Reg.	E452

Bus Transceivers

3-Bit Registered Bus XCVR	E336
3-Bit Scannable Reg. Bus XCVR	E337

Miscellaneous

Dual Analog Comparator w. Latch	E1651
Dual Analog Comparator w. Latch & Hysteresis	E1652
Programmable Delay Chip, Digital	E195
Programmable Delay Chip, Digital & Analog	E196
Hard Disk Data Separator	E197
1:4 Serial/Parallel Converter	E445
4:1 Parallel/Serial Converter	E446



This section contains a technical overview of the ECLinPS family as well as an outline of its electrical characteristics. In addition the section outlines the procedures and philosophies used to AC test the family.

CONTENTS

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SECTION 1
Family Overview

Introduction

Recent advances in bipolar processes have led to a proliferation of very high speed LSI and VLSI gate arrays in high end computer applications. The advent of these high speed arrays has created a need for a high speed logic family to tie or "glue" them together. Because arrays have a finite amount of circuitry and I/O pins, glue functions which are sensitive to either of these parameters may be better performed off of the array. In addition glue functions which require very tight skew control may be difficult to perform on an array due to the inherent skew of the large packages associated with large gate arrays. Therefore although the trend is to push more and more of the logic onto the array, there are design constraints which make performing some of the logic, such as clock distribution, multiplexing, decoding, latching, memory addressing and translating, in glue an attractive alternative.

The high end computer segment is not the only market segment pushing for higher performance logic parts. ATE, instrumentation and communication designs can have data rate requirements ranging from 300MHz to as high as 2.5GHz. Because large high speed arrays do not always lend themselves to passing high frequency signals on and off chip, portions of the designs must be realized with discrete logic. The current bipolar logic families are not capable of operating at these high frequencies.

To answer the call for a very high speed bipolar logic family Motorola has designed and produced the ECLinPS (ECL in Pico Seconds) logic family. The family was designed to meet the most stringent of system requirements in speed, skew and board density as well as maintaining compatibility to existing ECL families.

ECL Design Benefits

The speed benefits of an ECL design over those of alternative logic technologies are well documented, however there are a number of other important features that make ECL an attractive technology for system designs. The ECLinPS logic family as with other ECL families afford the following advantages:

Complimentary Outputs

Complimentary outputs are available on many functions with equal propagation delays between the two paths. This alleviates the need for external inverters and saves system power and board space while maintaining exceptional system timing.

Transmission Line Drive Capability

The low output impedance, high input impedance and high current drive capability of ECL makes it an ideal technology for driving transmission lines. Regardless of the technology, as system speeds increase, interconnect becomes more of a transmission line phenomenon. With ECL no special line driving devices are necessary as all ECL devices are line drivers.

Constant Power Supply Current Drain

Because of the differential amplifier design used for ECL circuits the current is not switched on and off but rather simply steered between two paths. Thus the current drain of an ECL device is independent of the logic state and the frequency of operation. This current stability greatly simplifies system power supply design.

Input Pulldown Resistors

ECL inputs have 50KΩ - 75KΩ internal pulldown resistors which pull the input to V_{EE} (logic LOW) when left open. This allows unused inputs to be left open and greatly simplifies logic design.

Differential Drive Capability

Because of the presence of high current drive complimentary outputs, ECL circuits are ideally suited for driving twisted pair lines or cables over long distances. With common mode noise rejection of 1V or more ECL line receivers are less susceptible to common mode noise. In addition their differential inputs need only a few hundred millivolt voltage differences to correctly interpret the logic.

High Speed Design Philosophy

Today a truly high speed logic family needs more than simply short propagation delays. The minimization of all types of skew as well as a level of logic density which affords a smaller amount of board space for an equivalent function are also necessities of a high speed family. The following summary will outline the steps taken by Motorola to achieve these goals in the development of the ECLinPS logic family.

Fast Propagation Delays

The ECLinPS family boasts 500ps maximum packaged

gate delays and typical flip flop toggle frequencies of 1.4GHz. Simple gate functions show typical propagation delays of 360ps at 25mW of power for a speed power product of only 9pJ. For higher density devices internal gates run at 100ps with 5mW of power for a speed power product of only .5pJ.

Internal Differential Interconnect

The propagation delay window size, skew between rising and falling inputs and susceptibility to noise are all phenomenon which are exacerbated by V_{BB} switching reference variation. By extensively using differential interconnects internal to the chip the ECLinPS family has been able to achieve superior performance in these areas.

Propagation Delay Temperature Insensitivity

The variation of propagation delay through an ECLinPS device across temperature is typically less than 50ps. This stability allows for faster designs due to tighter delay windows across temperature.

Input impedance and Loading Capacitance

The input structures of the ECLinPS family show a positive real impedance across the applicable input frequency range. This ensures that the system will remain stable and operate as designed over a wide range of input frequencies. The input loading capacitance typically measures only 1.5pF and is virtually independent of input fanout as the device capacitance is less than 5% of the total. Because the propagation delay of a signal down a transmission line is adversely affected by loading capacitance the overall system speed is enhanced.

Input Buffers

To minimize propagation delays in a system environment, inputs with a large internal fanout are buffered to minimize the loading capacitance on the transmission line.

High Level of Integration

28 pin designs allow for the design of 9 bit functions for implementation in byte plus parity applications. Full byte plus parity implementation reduces total package count and saves expensive board space.

Space Efficient Package

Surface mount PLCC package affords a high level of integration with a minimum amount of required board space. Quad layout of the package equalizes pin lengths thus minimizing the skew between similar internal paths.

Flow Through Pin Assignment

Input and output pins have been laid out in a flow through pattern with the inputs on one side of the package and the outputs on the other. This flow through pattern helps to simplify the PC board layout operation.

Multiple VCCO pins

To minimize the noise generated in simultaneous switching situations a minimum of three single ended outputs per V_{CCO} has been employed in the family. Optimum placement of these V_{CCO}'s also results in superior output to output skew.

Advanced Bipolar Processing

The ECLinPS logic family is fabricated using Motorola's MOSAIC III process, a process which is two generations ahead of the process used in the development of the 10KH family. The small geometries and feature sizes of the MOSAIC III process enables the ECLinPS logic family to boast of a nearly 3 fold improvement in speed at less than half the power of existing ECL logic families.

The MOSAIC III process is a double polysilicon process which uses a unique self-alignment scheme for device electrode and isolation definition. The process features self aligned submicron emitters as well as polysilicon base, collector and emitter electrodes. In addition polysilicon resistors, diodes and capacitors are available to minimize the parasitic capacitance of an ECL gate. Figure 1.1 shows a cross section for an NPN device using the MOSAIC III process.

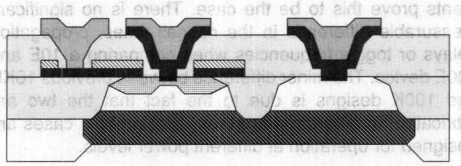


Figure 1.1 - MOSAIC III Cross Section

By incorporating the use of polysilicon contacts and resistors through the MOSAIC III process, the parasitic capacitances of an ECLinPS gate are minimized, thus minimizing the time constants which comprise the switching delays of the gate. The resultant gates show delays of 100ps for internal gates and 200ps for output gates capable of driving 50Ω loads. The small geometries of the process, nearly 350% reduction in device area compared to a 10KH device, allows these internal gate delays to be achieved at only 800μA of current.

Universal Compatibility

Each member of the ECLinPS family is available in both of the existing ECL standards: 10E series devices are compatible with the MECL 10KH family; 100E series devices are compatible with ECL 100K. In addition, to maintain compatability with temperature compensated, three level series gated gate arrays the 100E devices are guaranteed to

sion that there are inherent AC performance differences between them. In reality this is not the case. The only inherent difference between the two standards is the difference in the behavior of the DC characteristics with temperature.

AC Performance

From an IC design standpoint the only differences between a 10E device and a 100E device in the ECLinPS family is a small temperature compensation network in the 100E output gate, and very minimal differences in the two bias generator networks. Therefore one would expect that from an AC standpoint the performance of the two standards in the ECLinPS family should be nearly identical; measurements prove this to be the case. There is no significant measurable difference in the rise/fall times, propagation delays or toggle frequencies when comparing a 10E and 100E device. The minor difference between previous 10KH and 100K designs is due to the fact that the two are fabricated on different processes, and in some cases are designed for operation at different power levels.

Summary

Summarizing the above information; in general the two ECL design standards, although differing somewhat in DC parameters, are nearly identical when one compares the AC performance for a given device. There may be very small differences in the AC measurements due to the slightly smaller output swing of the 100E device. However these difference are negligible when compared to the absolute value of the measurements. Therefore from an AC standpoint there is no real advantage in using one standard over the other, thus removing AC performance as a decision variable in high speed system design.

Packaging

During the definition phase of the ECLinPS family much attention was placed on the identification of a suitable package for the family. The package had to meet the criteria of minimum parasitics and propagation delays along with an attractive I/O vs board space relationship. Although the DIP package offered a level of familiarity and convenience the performance of the package with a very high speed logic family was inadequate. In addition to the obvious parasitics tive in that it allows for a nearly 100% reduction in board space when compared to the DIP alternative. The package is approximately a half inch square with 50 mil spaced J-bend leads. More detailed measurements can be found in the package section of this databook. The J bend leads provide a smaller footprint than a gull wing package and propose fewer temperature expansion coefficient mismatch problems than the leadless alternative.

Thermally the standard PLCC exhibits a Θ_{JA} of 43.5°C per watt at 500 lfpm air flow. With this thermal resistance most 28 pin functions can be implemented with the MOSAIC III process without encountering any severe thermal problems. For more details on thermal issues of the ECLinPS family refer to the thermal section of this databook.

Abbreviation Definitions

The following is a list of abbreviations found in this databook and a brief definition of each.

Current

I_{CC} Total power supply current drawn from the positive supply by an ECLinPS unit under test.

I_{EE} Total power supply current drawn from an ECLinPS device under test by the negative supply.

I_{IL} Current drawn by the input of an ECLinPS device with a specified low level (VIL min) forced on the input.

I_{INH} Current drawn by the input of an ECLinPS device with a specified high level (VIH max) forced on the input.

I_{OUT} The current sourced by an output under specified load conditions.

Voltage

V_{BB} The switching reference voltage

V_{BE} Base-to-emitter voltage drop of a transistor at

specified collector and base currents.

V_{CB} Collector-to-base voltage drop of a transistor at specified collector and base currents.

V_{CC} The most positive supply voltage to an ECLinPS device.

V_{CCO} Power supply connection to the output emitter follower of an ECLinPS gate. For the ECLinPS logic family VCC and VCCO are common nodes.

V_{EE} The most negative supply voltage to an ECLinPS device.

V_{IH} Nominal input logic HIGH voltage level.

V_{IH} max Maximum (most positive) logic HIGH voltage level for which all parametric specifications hold.

V_{IH} min Minimum (least positive) logic HIGH voltage level for which all parametric specifications hold.

V_{IL} Nominal input logic LOW voltage.

V_{IL} max Maximum (most positive) logic LOW voltage level for which all parametric specifications hold.

V_{IL} min Minimum (least positive) logic HIGH voltage level for which all parametric specifications hold.

V_{OH} Output logic HIGH voltage level for the specified load condition.

V_{OHA} Output logic HIGH voltage level with the inputs biased at VIH min or VOL max.

V_{OH} max Maximum (most positive) logic HIGH output voltage level.

V_{OH} min Minimum (least positive) logic HIGH output voltage level.

V_{OL} Output logic LOW voltage level for the specified load condition.

V_{OLA} Output logic LOW voltage level with the inputs biased at VIH min or VOL max.

V_{OL} max Maximum (most positive) logic LOW output voltage level.

V_{OL} min Minimum (least positive) logic LOW output voltage level.

V_{TT} Output termination voltage for ECLinPS open emitter follower outputs.

V_{PP} Minimum peak to peak input voltage for differential input devices.

V_{CMR} The voltage range in which the logic HIGH voltage level of a differential input signal must fall for a differential input device.

V_{CUT} The logic LOW voltage level for ECL BUS outputs which attain cutoff of the output emitter follower.

V_{SUP} The maximum voltage difference between VEE and VCC for the E1651 comparator.

Timing Parameters

t_R Waveform rise time of an output signal measured from the 20% to 80% levels of the signal.

t_F Waveform fall time of an output signal measured from the 20% to 80% levels of the signal.

$T_{PD\pm\pm}$ Propagation delay of a signal measured for a rising/falling input to a rising/falling output.

xpt The crossing point of a differential input or output signal. The reference point for which differential delays are measured.

T_{PLH} The propagation delay for an output transitioning from a logic LOW level to a logic HIGH level.

T_{PHL} The propagation delay for an output transitioning from a logic HIGH level to a logic LOW level.

f_{MAX} Maximum input frequency for which an ECLinPS flip flop will function correctly.

f_{COUNT} Maximum input frequency for which an ECLinPS counter will function properly.

f_{SHIFT} Maximum input frequency for which an ECLinPS shift register will function properly.

t_{SKEW} The maximum delay difference between similar paths on a single ECLinPS device.

t_S Setup time; the minimum amount of time an input must transition before a clock transition to ensure proper function of the device.

t_H Hold time: the minimum amount of time an input must remain asserted after a clock transition to ensure proper operation of the device.

t_{RR} Release time or Reset Recovery Time; the mini

mum amount of time after a signal is de-asserted that a different input must wait before assertion to ensure proper functionality of the device.

t_W min — Minimum pulse width of a signal necessary to ensure proper functionality of a device.

Temperature

T_{STG} — The maximum temperature at which a device may be stored without damage or performance degradation.

T_J — Junction (or die) temperature of an integrated circuit device.

T_A — Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit package.

Θ_{JA} — Thermal resistance of an integrated circuit package between the junction and the ambient.

Θ_{JC} — Thermal resistance of an integrated circuit package between the junction and the case.

Θ_{CA} — Thermal resistance of an integrated circuit package between the case and the ambient.

lfpm — Linear feet per minute.

Miscellaneous

D.U.T. — Device under test.

C_{IN} — Input capacitance of a device.

Z_{IN} — Input impedance of a device.

C_{OUT} — Output capacitance of a device.

Z_{OUT} — Output impedance of a device.

P_D — The total dc power applied to a device, not including any power delivered from the device to the load.

R_L — Load resistance

R_T — Transmission line termination resistor.

R_P — An input pull-down resistor.

P.U.T. — Pin under test.

SECTION 2
Electrical Characteristics

DC Characteristics

ECLinPS Transfer Curves

As mentioned in the previous section, except for the E1651, E1652 and E197 all ECLinPS devices are offered in either 10E or 100E versions to be compatible with 10KH or 100K ECL logic respectively. The following information will overview the DC characteristics of the two versions of ECLinPS devices, for more detailed discussions the reader is referred to the MECL and F100K databooks.

Both 10E and 100E devices produce ≈800mV output swings into a specified 50Ω to -2.0V load. However because of the low output impedance (Figure 2.1) of both standards neither is limited to 50Ω loads. Larger load resistances can be used to reduce the system power without sacrificing the speed of the device. Of course the overall system speed will be reduced due to the increased delays of the interconnect traces. In addition, to better drive high capacitive lines, smaller resistances, down to 25Ω, can be used without violating the 50mA max output current specification. It is however recommended that for lines of less than 35Ω specialized 25Ω driver circuits or "ganged" output schemes should be used to ensure optimum long term reliability of the device.

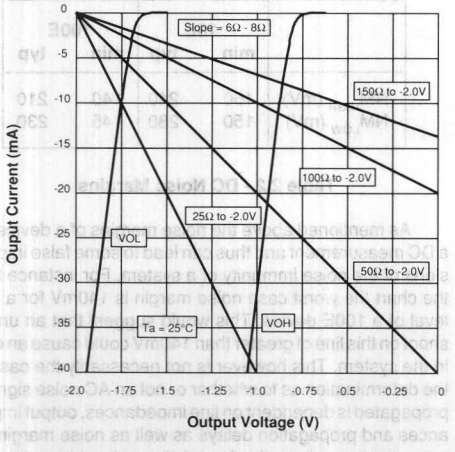


Figure 2.1 - Output Characteristics vs Load

The 10E devices are voltage compensated but not temperature compensated, therefore although the output voltage levels are insensitive to variations in V_{EE} they do vary with temperature. The transfer curves in Figure 2.2 pictorially illustrate the behavior of the 10E outputs. In order to maintain noise margins over temperature it is important that the V_{BB} switching reference tracks with temperature in such a way as to remain centered between the V_{OH} and V_{OL} levels. As shown in Table 2.1 the temperature tracking rates of the V_{OH} and V_{OL} for a 10E device are not equal. Therefore it is

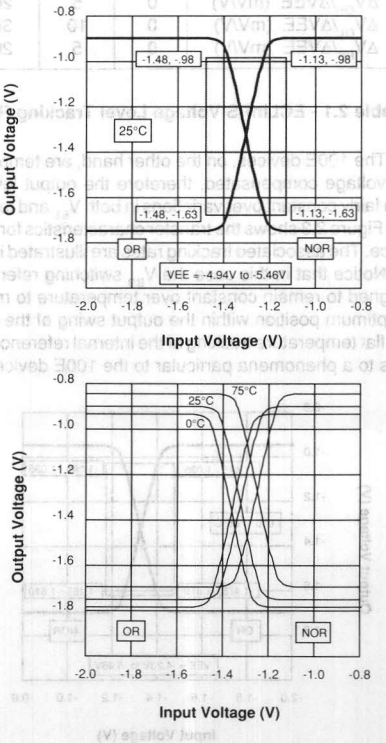


Figure 2.2 - ECLinPS 10E Transfer Curves

$\Delta V_{OH}/\Delta VEE$ (mV/V)	0	5	20
$\Delta V_{OL}/\Delta VEE$ (mV/V)	0	10	30
$\Delta V_{BB}/\Delta VEE$ (mV/V)	0	5	20

100E	min	typ	max
$\Delta V_{OH}/\Delta T$ (mV/°C)	-.15	0	.15
$\Delta V_{OL}/\Delta T$ (mV/°C)	-.30	0	.30
$\Delta V_{BB}/\Delta T$ (mV/°C)	-.20	0	.20
$\Delta V_{OH}/\Delta VEE$ (mV/V)	0	5	20
$\Delta V_{OL}/\Delta VEE$ (mV/V)	0	10	30
$\Delta V_{BB}/\Delta VEE$ (mV/V)	0	5	20

Table 2.1 - ECLinPS Voltage Level Tracking Rates

The 100E devices, on the other hand, are temperature and voltage compensated, therefore the output levels remain fairly constant over variations in both V_{EE} and temperature. Figure 2.3 shows the transfer characteristics for a 100E device. The associated tracking rates are illustrated in Table 2.1. Notice that in this case the V_{BB} switching reference is designed to remain constant over temperature to maintain an optimum position within the output swing of the device. This flat temperature tracking of the internal reference levels leads to a phenomena particular to the 100E devices.

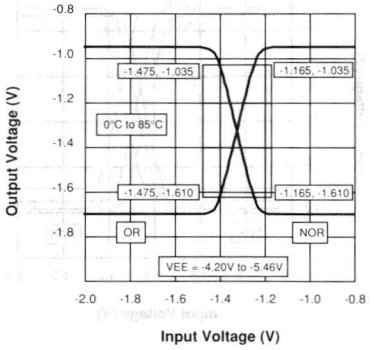


Figure 2.3- ECLinPS 100E Transfer Characteristics

characteristics. Both designs show superior I_{EE} vs V_{EE} tracking rates due to the design of the voltage regulator. With a tracking rate of <3%/V this variation can effectively be ignored during system design. The output level and reference level variation with V_{EE} are also outstanding as can be seen in Table 2.1.

Noise Margin

The noise margin of a device is a measure of a device's resistance to undesirable switching. For ECLinPS as well as all ECL devices, noise margin is a DC specification. The noise margin is defined as the difference between the voltage level of an output of the sending device and the required voltage level of the input of the receiving device. Therefore a worst case noise margin can be calculated from the ECLinPS data sheets by simply subtracting the V_{IL} max or V_{IH} min from the V_{OL} min or V_{OH} max respectively. Table 2.2 below illustrates the worst case and typical noise margins for both 10E and 100E ECLinPS devices. Notice that the typical noise margins are approximately 100mV larger than the worst case.

	10E		100E	
	min	typ	min	typ
NM_{HIGH} (mV)	150	240	140	210
NM_{LOW} (mV)	150	280	145	230

Table 2.2 - DC Noise Margins

As mentioned above the noise margins of a device are a DC measurement and thus can lead to some false impressions of the noise immunity of a system. For instance from the chart the worst case noise margin is 140mV for a high level of a 100E device. This would suggest that an undershoot on this line of greater than 140mV could cause an error in the system. This however is not necessarily the case as the determination as to whether or not an AC noise signal is propagated is dependent on line impedances, output impedances and propagation delays as well as noise margins. A more thorough investigation of the noise immunity of a system can be found in Application Note AN-592.

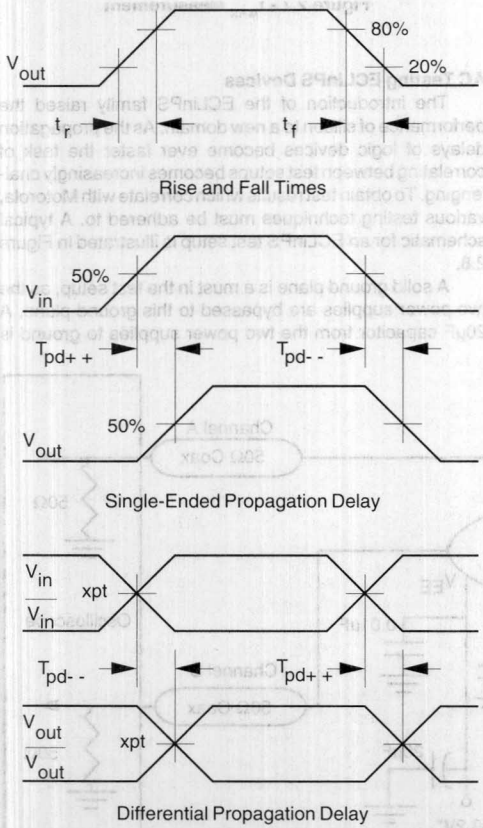


Figure 2.4 - ECLinPS T_{PD} Measurement Waveforms

Propagation delays and rise/fall times are generally well understood parameters, however there is sometimes confusion surrounding the definitions of more specialized AC engineer to obtain actual evaluation data if this parameter is critical in their designs.

Set-Up and Hold Times

Motorola defines the setup time of a device as the minimum time, prior to the transition of the clock, that an input must be stable to ensure that the device operates properly. The hold time, on the other hand, is defined as the minimum time that an input must remain stable after the transition of the clock to ensure that the device operates properly. Figure 2.5 illustrates the way in which Motorola defines setup and hold times.

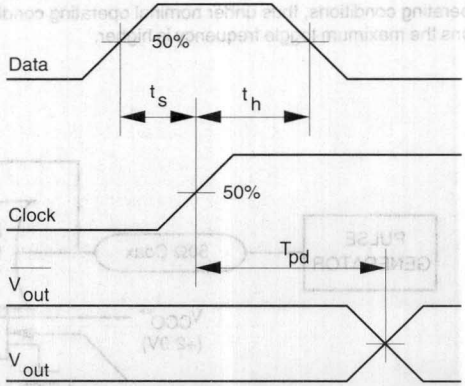


Figure 2.5 - Set-Up and Hold Waveforms

Release Times

Release times are defined as the minimum amount of time an input must wait to be clocked after an enable, master reset or set signal is deactivated to ensure proper operation. Because more times than not this specification is in reference to a master reset operation this parameter is often called reset recovery time. Figure 2.6 illustrates the definition of release time in the Motorola data sheets.

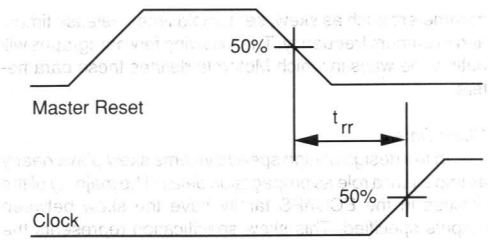


Figure 2.6 - ECLinPS Release Time Waveforms

f_{MAX} Measurement

In general f_{MAX} is measured in the manner shown in Figure 2.7 with the fail criterion being either a swing of 600mV or less, or a miscount. However in some cases the feedback method of testing can lead to a pessimistic value of f_{MAX} because the feedback path delay is such that the setup times of the device are violated. If this is the case it is necessary to have two free running signal generators to ensure that the setup times are observed. This parameter, along with f_{SHIFT} and f_{COUNT}, represents the maximum frequency at which a particular flip flop, shift register or counter can be clocked with the divide, shift or count operation guaranteed. This number is generated from worst case operating conditions, thus under nominal operating conditions the maximum toggle frequency is higher.

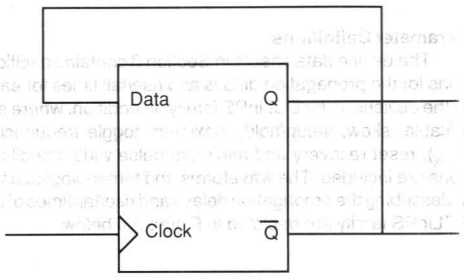
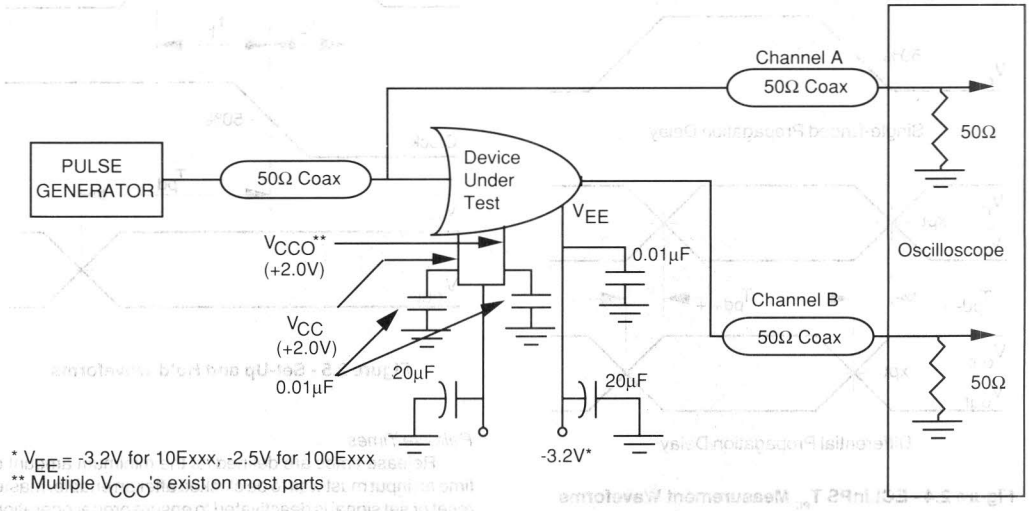


Figure 2.7 - f_{MAX} Measurement

AC Testing ECLinPS Devices

The introduction of the ECLinPS family raised the performance of silicon to a new domain. As the propagation delays of logic devices become ever faster the task of correlating between test setups becomes increasingly challenging. To obtain test results which correlate with Motorola, various testing techniques must be adhered to. A typical schematic for an ECLinPS test setup is illustrated in Figure 2.8.

A solid ground plane is a must in the test setup, as the two power supplies are bypassed to this ground plane. A 20µF capacitor from the two power supplies to ground is



* V_{EE} = -3.2V for 10Exxx, -2.5V for 100Exxx

** Multiple V_{CCO}'s exist on most parts

Figure 2.8 - Typical ECLinPS Test Setup

20μF capacitor from the two power supplies to ground is used to dampen any supply variations. An RF quality .01μF capacitor from each power pin to ground is used to decouple the fixture. These .01μF capacitors should be located as close to the power pins of the package as possible. In addition, in order to minimize the inductance of the power pins, all of the power leads should be kept as short as possible. The power supplies are shifted by +2.0V so that the load comprises only the precision 50Ω input impedance of the oscilloscope. Use of this technique will assure that the customer and Motorola are terminating devices into equivalent loads and will improve test correlation.

To further standardize testing any unused outputs should be loaded with 50Ω to ground.

Because the power supplies are shifted, the input levels must also be shifted by an equal amount. Table 2.3 gives the typical input levels for the ECLinPS family and their corresponding +2.0V shifted levels.

10Exxx	Typical	Shifted
V_{IL}	-1.75V	+0.25V
V_{IH}	-0.90V	+1.10V
100Exxx	**Typical**	**Shifted**
V_{IL}	-1.70V	+0.30V
V_{IH}	-0.95V	+1.05V

Table 2.3 - ECL Levels after Translating by +2.0V

The test fixture should be in a controlled impedance 50Ω environment, with any non-50Ω interconnects, or stubs, kept as short as possible (<1/4"). This controlled impedance environment will help to minimize overshoot and ringing, two phenomena which can lead to inaccuracies in AC measurements. To minimize degradation of the input and output edge rates a 50Ω coaxial cable with a teflon dielectric is recommended, however any other cable with a bandwidth of >5.0GHz is adequate. In addition, the cables from the device under test (DUT) to the inputs of the scope should be matched in length to prevent any errors due to different path lengths from the DUT to the scope. The interconnect fittings should be 50Ω SMA straight or SMA launchers to minimize impedance mismatches at the interface of the coax and test PC board. Although a teflon laminate board is preferable, an FR4 laminate board is acceptable as long as the signal traces are kept to five inches or less. Longer traces will result in significant edge rate degradation of the input and output signals.

To make the board useful for incoming inspection or other volume testing the board needs to be fitted with a socket. Although not suitable for AC testing due to different pin lengths and large parasitics, there are through hole sockets which are adequate for DC testing of ECLinPS devices. For AC testing purposes a 28 pin PLCC surface mount socket is recommended. At the publication of this databook there are two sockets available which the Motorola ECLinPS group recommends: AMP part # 822039-1 and Method Electronics part #'s 213-028-601 or 213-028-602.

To ease the correlation issue Motorola has developed a universal AC test board which is now available to customers. The board is fitted with a PLCC socket and comes with instructions on how it can be configured for the different device types in the family. For ordering information see the description on the following page.

Finally, to ensure correlation between Motorola and the customer, high performance state-of-the-art measuring equipment should be used. The pulse generator must be capable of producing the required input levels with rise and fall times of 500ps. In addition, if f_{MAX} is going to be tested, a frequency of of up to 1.5GHz may be needed. The oscilloscope should also be of the utmost in performance with a minimum bandwidth of 5.0 GHz.

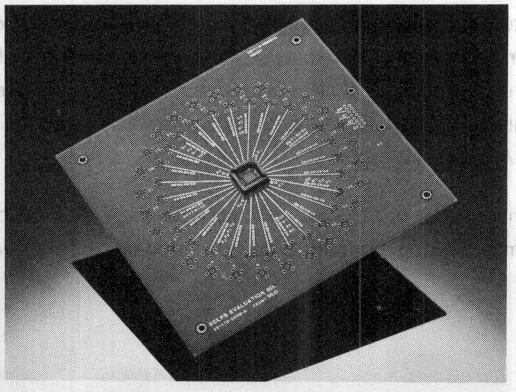


Figure 2.9 — ECLinPS AC Test Board

Product Family. The board provides a high bandwidth 50 ohm controlled impedance environment. The board is universal and can be configured by the user for any of the 28 pin PLCC devices in the family depending on the input, output, and power pinout layout of the device. The table below indicates common input/output/power devices.

Group	Base Device	Pin Compatible Devices
CONF1	E196	E195
CONF2	E142	E016,E141,E143,E241
CONF3	E337	E336
CONF4	E212	E104,E107,E150,E151
CONF5	E156	E155,E167,E171,E256
CONF6	E158	E116,E122,E175,E416
CONF7	E154	E452
CONF8	E101	E131,E157,E404
CONF9	E112	
CONF10	E431	E457
CONF11	E111	
CONF12	E164	E160
CONF13	E451	
CONF14	E163	E166
CONF15	E193	

Table 1: Cross Reference of Board Configuations

The board is designed to test devices using the fly-by (Kelvin contact) test method, therefore one input force trace and one input sense trace exists for each input pin. This allows termination of the input and output signals into the highly accurate 50 ohm impedance of an oscilloscope. The layout is engineered to have equal length traces from the device under test (DUT) socket to the sense outputs which simplifies the calibration requirements for accurate AC measurements.

The kit provides a printed circuit board with an attached surface mount socket as well as assembly instructions. For superior impedance control from the cable to the board, Motorola recommends the use of SMA coaxial connectors.

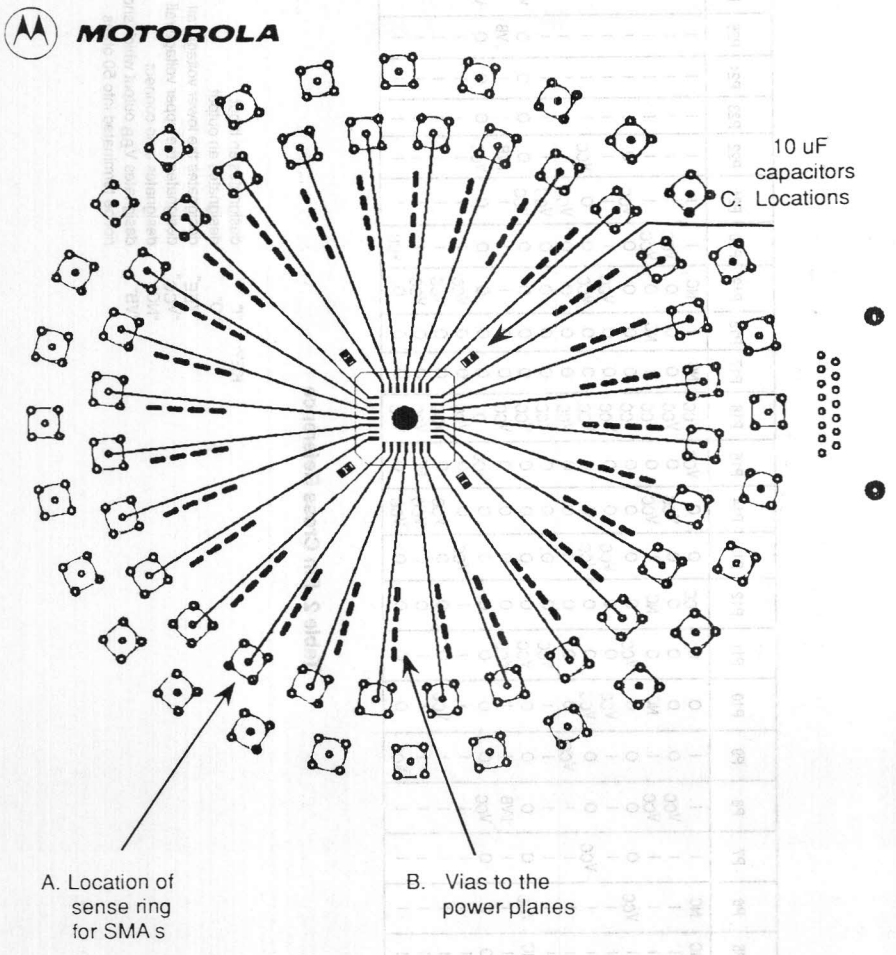


Figure 1. Front View of ECLinPS Evaluation Board

Group	Part(s)	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	# of Connectors
CONF1	E196	V_{EE}	I	I	VB	NC	NC	I	I	I	O	O	V_{CC}	O	O	V_{CC}	V_{CC}	NC	I	NC	I	I	I	I	I	I	I	I	I	35
CONF2	E142	V_{EE}	I	I	I	I	I	I	V_{CC}	O	O	O	O	O	V_{CC}	O	V_{CC}	O	O	O	V_{CC}	I	I	I	I	I	I	I	I	I	37
CONF3	E337	V_{EE}	I	I	I	I	I	I	V_{CC}	I	NC	O	NC	I	V_{CC}	O	V_{CC}	I	NC	O	V_{CC}	I	I	I	I	I	I	I	I	I	37
CONF4	E212	V_{EE}	I	I	I	I	V_{CC}	O	O	O	O	V_{CC}	O	O	O	O	V_{CC}	O	O	O	O	V_{CC}	O	I	I	I	I	I	I	I	33
CONF5	E156	V_{EE}	I	I	I	I	I	I	I	I	V_{CC}	O	O	V_{CC}	O	O	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	I	I	I	I	40
CONF6	E158	V_{EE}	I/VB	I	I	I	I	V_{CC}	O	O	V_{CC}	O	O	V_{CC}	O	O	V_{CC}	O	O	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	I	32
CONF7	E154	V_{EE}	I/VB	I	I	I	I	I	I	V_{CC}	O	O	O	O	O	O	V_{CC}	O	O	O	O	V_{CC}	I	I	I	I	I	I	I	I	38
CONF8	E101	V_{EE}	I	I	I	I	I	I	I	I	I	V_{CC}	O	O	O	O	V_{CC}	O	O	O	O	V_{CC}	I	I	I	I	I	I	I	I	40
CONF9	E112	V_{EE}	I	I	I	NC	V_{CC}	O	O	O	O	V_{CC}	O	O	O	O	V_{CC}	O	O	O	O	V_{CC}	O	O	O	O	V_{CC}	I	I	I	26
CONF10	E431	V_{EE}	I/VB	I	I	I	I	I	I/VB	I	I	V_{CC}	O	O	O	O	V_{CC}	O	O	I	I	I	I/VB	I	I	I/VB	I	I	I	I	44
CONF11	E111	V_{EE}	I	VB	NC	O	O	O	V_{CC}	O	O	O	O	O	O	V_{CC}	O	O	O	O	O	O	V_{CC}	O	O	O	V_{EE}	I	I	25
CONF12	E164	V_{EE}	I	I	I	I	I	I	I	I	I	I	I	V_{CC}	O	O	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	I	I	I	44
CONF13	E451	V_{EE}	I	NC	I	I	I	I	I	I	V_{CC}	O	O	O	V_{CC}	O	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	I	VB	I	37
CONF14	E163	V_{EE}	I	I	I	I	I	I	I	I	I	I	O	O	V_{CC}	NC	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	I	I	I	42
CONF15	E193	V_{EE}	I	I	I	I	I	I	I	V_{CC}	O	O	O	O	V_{CC}	O	V_{CC}	O	O	O	V_{CC}	I	I	I	I	I	I	I	I	I	38

Table 2. Pin Cross Reference

KEY:
- "I" designates an input
- "O" designates an output
- "V_{EE}" designates the lower voltage rail
- "V_{CC}" designates the upper voltage rail
- "NC" designates a no connect
- "VB" designates V_{BB} output which should not be terminated into 50 ohms

ASSEMBLING THE ECLinPS EVALUATION BOARD

The evaluation board is designed for characterizing devices in a laboratory environment using high bandwidth sampling oscilloscopes such as the Hewlett Packard 54120T, the Tektronix 11800 Series, or the Tektronix 7854. The board is designed using Kelvin contact (fly-by) techniques to present the input signals to the DUT. Each pin on the board has two traces, one force and one sense. Inputs pins use one force and one sense line, while outputs need only a sense line. This means that input signals are terminated through the sense line into the 50 ohm input of a sampling oscilloscope instead of at the input to the DUT. Please refer to the AC Testing section of the ECLinPS Data Book for further information and a simplified figure of the test setup.

The first step in building a board is determining which input/output/power configuration is necessary for the device of interest. Table 1 on the first page of the Applications Information shows all the board configurations. For example, if the devices of interest were the E104 and the E151, then CONF2 would be selected. Table 2 is a pin cross reference for each configuration.

I. Installing the SMA Connectors

Table 2 indicates the number of SMA connectors needed to populate an evaluation board for a given configuration. Depending on the device and the parameters of interest, it may not be necessary to install the full complement of SMA connectors. For example, some devices have two clock inputs or common clocks and individual clocks. Figure 1 is the front view of the ECLinPS evaluation board. Item A points to the inner ring which connects to the sense traces of the DUT. The outer ring connects to the force traces. An input requires one SMA connector for the force and one SMA connector for the sense, while an output only requires a connection to the sense trace. Insert all the SMA connectors into the board and solder to the board. A simple assembly technique is to place a stiff piece of cardboard (8" x 7" or larger) on top of all the connectors and hold the board and cardboard together. Invert the board, place on a level surface, and all the connectors will be seated properly and can be soldered in place.

II. Connecting Power Planes to DUT Socket

There are four voltage planes on the ECLPSBD28. One is dedicated to ground and the other three: B1, B2, B3 are uncommitted. These planes are accessible through a power connection and sets of four vias that are adjacent to each sense trace. This is identified as Item B in Figure 1. For standard parts, B1 can be assigned V_{CC}, B2 can be assigned to V_{EE}, and B3 can be assigned to ground. Table 2 indicates which pins need to be connected to the various supply voltages. On the front side of the board, solder a jumper wire from the closest V_{EE} or V_{CC} via to the sense trace for each V_{CC}, V_{CCO}, and V_{EE} pin. Near the DUT there are sets of ground/bias plane vias that accommodate power supply decoupling capacitors. These are identified as Item C. On the front side of the board install 10 μF capacitors and on the back side install a 0.01 μF high frequency capacitor in parallel to decouple the V_{EE} and V_{CC} planes.

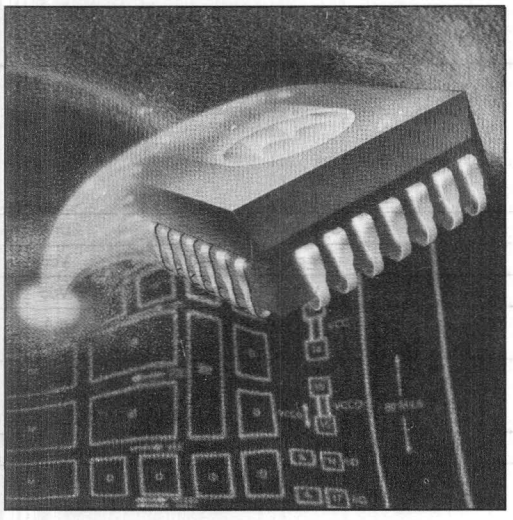
III. Cutting Force Traces for Outputs

Because of the design of the board all force traces for output pins will appear as transmission line stubs connected to the output pin. On the back side of the board, cut the force traces associated with the outputs using a razor blade knife. It is important to cut the trace very close to the DUT area to minimize the stub length. Also cut the force traces that are connected to V_{CC}, V_{CCO}, and V_{EE} pins.

IV. Installing the Chip Capacitors for the V_{CC}/V_{CCO} Pins

In the kit are 0.01 μF chip capacitors for use in decoupling the V_{CC} and V_{CCO} pins to the ground plane. This is critical because the power pins are not directly connected to the V_{CC} plane as in an actual board layout. On the back side of the board beneath the DUT socket are pads for each pin which allow connection of chip capacitors to the center island (GND) for each V_{CC} and V_{CCO} pin. Stand the chip capacitors on edge when soldering them in place so that adjacent pins are not shorted together.

299 Johnson Ave. P.O. Box 1249 Waseca, Minnesota 56093 (800)-247-8343 or (507)-835-6222	Jack Receptacle 142-0701-201
MACOM Omni Spectra 140 Fourth Avenue Waltham, Massachusetts 02254 (617)-890-4750	0.200" PC Mount SMA Straight Jack 2062-0000-00



ECLinPS Family Specifications & Device Data Sheets

3

This section contains AC & DC specifications for each ECLinPS device type. Specifications common to all device types can be found in the first part of this section. While specifications unique to a particular device can be found in the individual data sheets following the family specifications.

Data Sheet Classification

Advance Information — product in the sampling or pre-production stage at the time of publication.

Product Preview — product in the design stage at the time of publication.

Absolute Maximum Ratings

Beyond which device life may be impaired.[1]

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0 V)	V_{EE}	−8 to 0	Vdc
Input Voltage (V_{CC} = 0 V)	V_I	0 to −6 V	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range 10E Series 100E Series	T_A	 0 to +75 0 to +85	°C
Operating Range[2]	V_{EE}	−5.7 to −4.2	V

1. Unless specified otherwise on individual data sheet.
2. Parametric values specified at: 100E series: −4.2 V to −5.46 V
   10E series: −4.94 V to −5.46 V

10E Series DC Characteristics

V_{EE} = −5.2 V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Characteristic	0°C		25°C		75°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	−1020	−840	−980	−810	−920	−735	−910	−720	mV
V_{OL}	Output LOW Voltage	−1950	−1630	−1950	−1630	−1950	−1600	−1950	−1595	mV
V_{IH}	Input HIGH Voltage	−1170	−840	−1130	−810	−1070	−735	−1060	−720	mV
V_{IL}	Input LOW Voltage	−1950	−1480	−1950	−1480	−1950	−1450	−1950	−1445	mV
I_{IL}	Input LOW Current	0.5		0.5		0.3		0.3		μA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 volts, except bus outputs which, where specified, are terminated into 25 Ω.

100E Series DC Characteristics

V_{EE} = −4.2 V to −5.46 V; V_{CC} = V_{CCO} = GND; T_A = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV		
V_{OHA}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLA}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5			μA	V_{IN} = $V_{IL(min)}$	

This table replaces the three tables at different supply voltages in the previous edition and in ECL 100K literature. The same DC parametric values at V_{EE} = −4.5 V now apply across the full V_{EE} range of −4.2 to −5.46 V.

MC10E016
MC100E016

8-BIT SYNCHRONOUS BINARY UP COUNTER

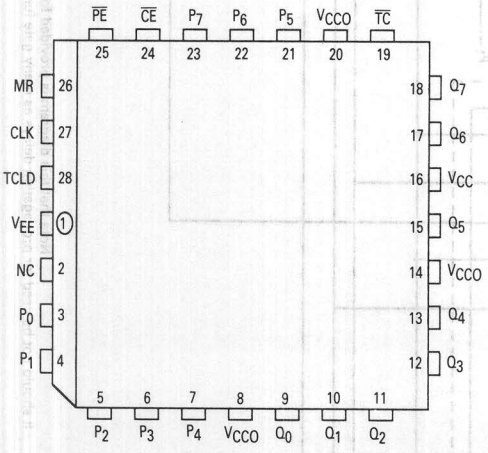
3

- 700 MHz Min. Count Frequency
- 1000 ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

The MC10E/100E016 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the MC10H016 in the MECL 10KH family, extended to 8-bits, as shown in the logic symbol.

The counter features internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all-one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically re-load upon $\overline{TC}$ = LOW, thus functioning as a programmable counter.

PINOUT: 28-LEAD PLCC (TOP VIEW)



FUNCTION TABLE

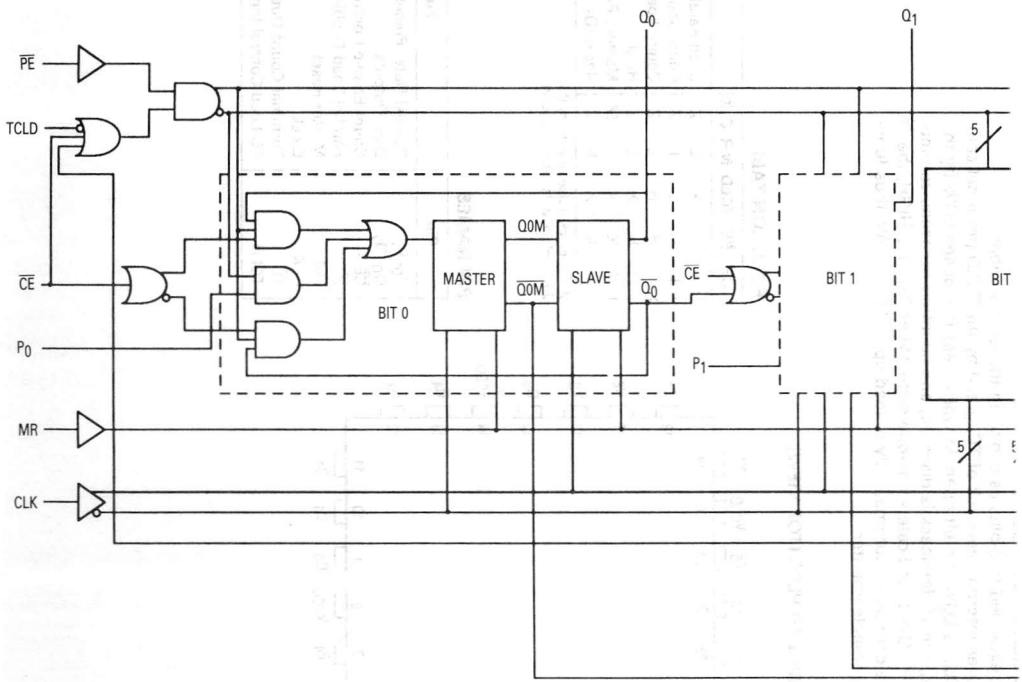
$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	Function
X	L	X	L	Z	Load Parallel (P_n to Q_n)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	Z	Reset (Q_n := LOW, $\overline{TC}$:= HIGH)

Z = clock pulse (low to high);
ZZ = clock pulse (high to low)

PIN NAMES

Pin	Function
P_0–P_7	Parallel Data (Preset) Inputs
Q_0–Q_7	Data Outputs
$\overline{CE}$	Count Enable Control Input
$\overline{PE}$	Parallel Load Enable Control Input
MR	Master Reset
CLK	Clock
$\overline{TC}$	Terminal Count Output
TCLD	TC-Load Control Input

8-BIT BINARY COUNTER LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation onl
It should not be used for propagation delays as many gate functions are achieved internally without

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		151	181		151	181		151	181		
	100E		151	181		151	181		174	208		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
f_{COUNT}	Max. Count Frequency	700	900		700	900		700	900		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	CLK to Q	600	725	1000	600	725	1000	600	725	1000		
	MR to Q	600	775	1000	600	775	1000	600	775	1000		
	CLK to $\overline{TC}$ (Q's loaded)	550	775	1050	550	775	1050	550	775	1050		1
	CLK to $\overline{TC}$ (Q's unloaded)	550	700	900	550	700	900	550	700	900		1
	MR to $\overline{TC}$	625	775	1000	625	775	1000	625	775	1000		
t_s	Setup Time										ps	
	Pn	150	-30		150	-30		150	-30			
	CE	600	400		600	400		600	400			
	PE	600	400		600	400		600	400			
	TCLD	500	300		500	300		500	300			
t_h	Hold Time										ps	
	Pn	250	30		250	30		250	30			
	CE	0	-400		0	-400		0	-400			
	PE	0	-400		0	-400		0	-400			
	TCLD	100	-300		100	-300		100	-300			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width										ps	
	CLK, MR	400			400			400				
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	510	800	300	510	800	300	510	800		

1. CLK to $\overline{TC}$ propagation delay is dependent on the loading of the Q outputs. With all of the Q outputs loaded the noise generated in going from a IIII IIII state to a 0000 0000 state causes the CLK to $\overline{TC}$+ delay to increase

FUNCTION TABLE

FUNCTION	$\overline{PE}$	$\overline{CE}$	MR	TCLD	CLK	P7-P4	P3	P2	P1	P0	Q7-Q4	Q3	Q2	Q1	Q0	$\overline{TC}$
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Count	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Hold	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
Load On	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H
Terminal	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H
Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H

3

Applications Information

Cascading Multiple E016 Devices

For applications which call for larger than 8-bit counters multiple E016's can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of E016 devices. Two E016's can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

Figure 1 below pictorally illustrates the cascading of 4 E016's to build a 32-bit high frequency counter. Note the E101 gates used to OR the terminal count outputs of the lower order E016's to control the counting operation of the higher order bits. When the terminal count of the preceeding device (or devices) goes low (the counter reaches an all 1's state) the more significant E016 is set in its count mode and will count one binary digit upon the next positive clock transistion. In addition, the preceeding devices will also count one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an E016 in the chain to count all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting E016 devices from Figure 1 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for the cascaded counter chain is set by the propagation delay of the $\overline{TC}$ output and the necessary setup time of the $\overline{CE}$ input and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the $\overline{TC}$ propagation delay and the $\overline{CE}$ setup time). Figure 1 shows E101 gates used to control the count enable inputs, however if the frequency of operation is lower a slower ECL OR gate can be used. Using the worst case guarantees for these parameters from the ECLinPS data book the maximum count frequency for a greater than 16-bit counter is 475MHz and that for a 16-bit

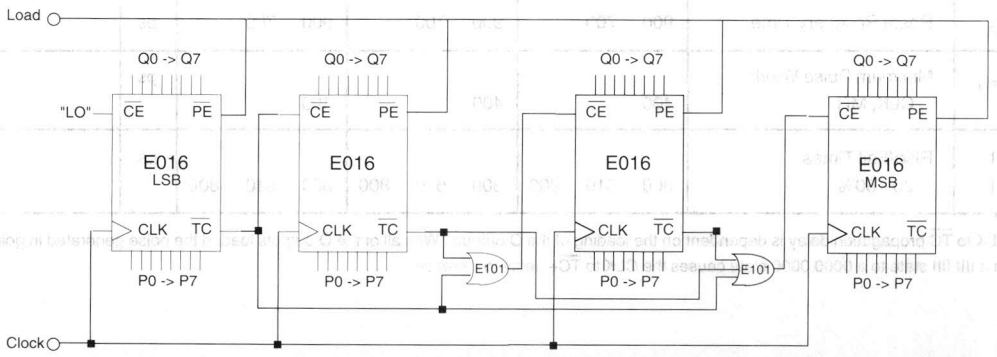


Figure 1 - 32-Bit Cascaded E016 Counter

Applications Information

counter is 625MHz. Note that this assumes the trace delay between the $\overline{TC}$ outputs and the $\overline{CE}$ inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.

Programmable Divider

The E016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1's state on the outputs). Because this feedback is built internal to the chip the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 2 below illustrates the input conditions necessary for utilizing the E016 as a programmable divider set up to divide by 113.

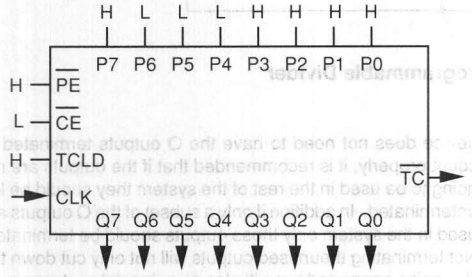


Figure 2 - Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

$Pn's = 256 - 113 = 8F_{16} = 1000\ 1111$

where:

P0 = LSB and P7 = MSB

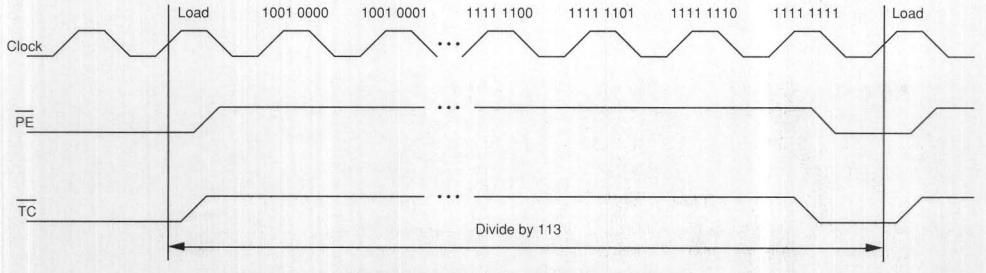
Forcing this input condition as per the setup in Figure 2 will result in the waveforms of Figure 3. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the E016 and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Divide Ratio	Preset Data Inputs P7	P6	P5	P4	P3	P2	P1	P0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

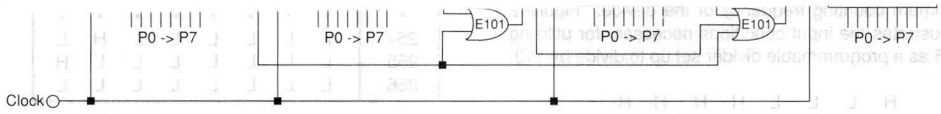
Table 1 - Preset Values for Various Divide Ratios

A single E016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple E016's can be cascaded in a manner similar to that already discussed. When E016's are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters untill all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple E016 divider chains.

Figure 4 on the following page shows a typical block diagram of a 32-bit divider chain. Once again to maiximize the frequency of operation E101 OR gates were used. For lower frequency applications a slower OR gate could replace the E101. Note that for a 16-bit divider the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant E016 must also feed the $\overline{CE}$ input of the most significant E016. If the two $\overline{TC}$ outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$



Divide by 113 E016 Programmable Divider Waveforms



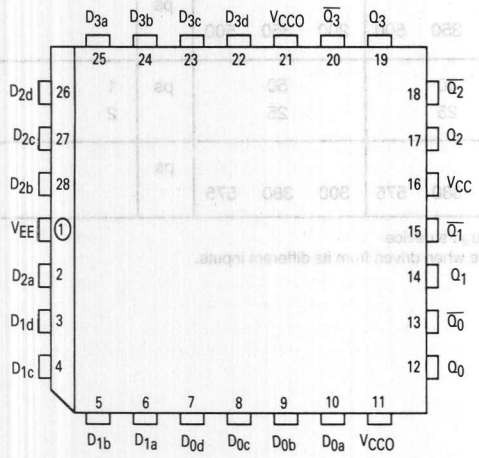
32-Bit Cascaded E016 Programmable Divider

feedback is external and requires external gating the maximum frequency of operation will be significantly less than the same operation in a single device.

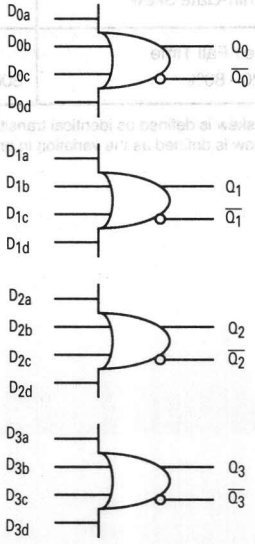
Maximizing E016 Count Frequency

The E016 device produces 9 fast transitioning single ended outputs, thus V_{CC} noise can become significant in situations where all of the outputs switch simulataneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating theunused outputs will not only cut down the V_{CC} noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_{0a}–D_{3d}	Data Inputs
Q_0–Q_3	True Outputs
$\overline{Q_0}$–$\overline{Q_3}$	Inverting Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		30	36		30	36		30	36		
	100E		30	36		30	36		35	42		

3

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	200	350	500	200	350	500	200	350	500	ps	
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_{SKEW}	Within-Gate Skew		25			25			25			2
t_r t_f	Rise / Fall Time 20 - 80%	300	380	575	300	380	575	300	380	575	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device
2. Within-gate skew is defined as the variation in propagation delays of a gate when driven from its different inputs.

MC10E104
MC100E104

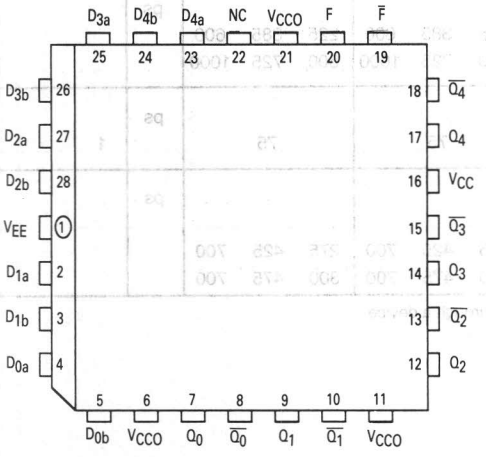
- 600 ps Max. Propagation Delay
- OR/NOR Function Outputs
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

QUINT 2-INPUT AND/NAND GATE

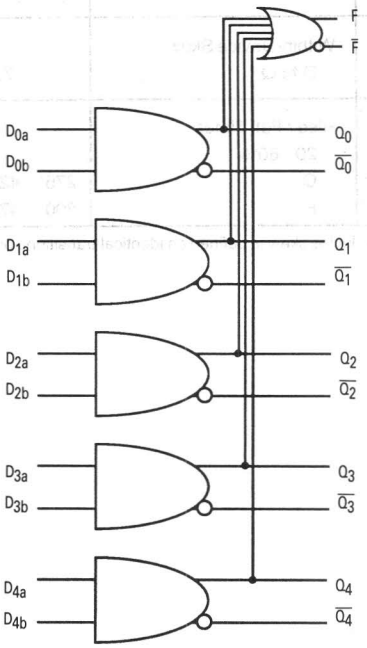
3

The MC10E/100E104 is a quint 2-input AND/NAND gate. The function output F is the OR of all five AND gate outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_{0a}–D_{4b}	Data Inputs
Q_0–Q_4	AND Outputs
$\overline{Q_0}$–$\overline{Q_4}$	NAND Outputs
F	OR Output
$\overline{F}$	NOR Output

FUNCTION OUTPUTS

$$F = (D_{0a} \cdot D_{0b}) + (D_{1a} \cdot D_{1b}) + (D_{2a} \cdot D_{2b}) + (D_{3a} \cdot D_{3b}) + (D_{4a} \cdot D_{4b})$$

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	D to Q	225	385	600	225	385	600	225	385	600		
	D to F	500	725	1000	500	725	1000	500	725	1000		
t_{SKEW}	Within-Device Skew										ps	
	D to Q		75			75			75			1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%											
	Q	275	425	700	275	425	700	275	425	700		
	F	300	475	700	300	475	700	300	475	700		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E107
MC100E107

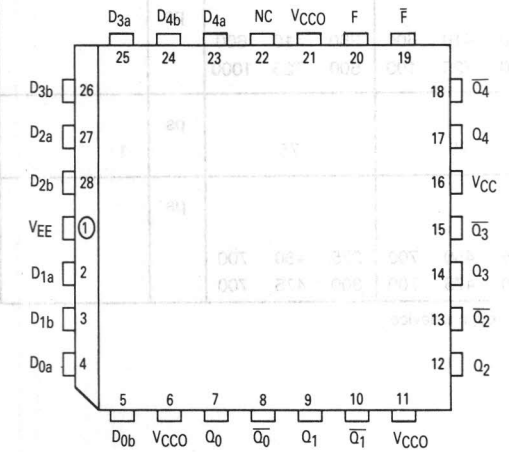
- 600 ps Max. Propagation Delay
- OR/NOR Function Outputs
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

QUINT 2-INPUT XOR/XNOR GATE

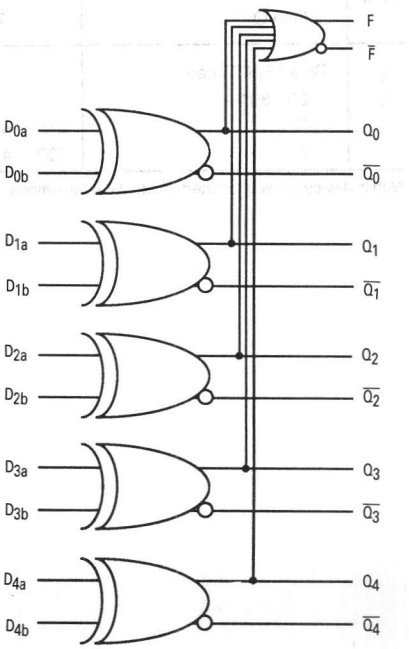
3

The MC10E/100E107 is a quint 2-input XOR/XNOR gate. The function output F is the OR of all five XOR outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_{0a}–D_{4b}	Data Inputs
Q_0–Q_4	XOR Outputs
$\overline{Q_0}$–$\overline{Q_4}$	XNOR Outputs
F	OR Output
$\overline{F}$	NOR Output

FUNCTION OUTPUTS

$$F = (D_{0a} \oplus D_{0b}) + (D_{1a} \oplus D_{1b}) + (D_{2a} \oplus D_{2b}) + (D_{3a} \oplus D_{3b}) + (D_{4a} \oplus D_{4b})$$

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			200			200			200	µA	
I_{EE}	Power Supply Current										mA	
	10E		42	50		42	50		42	50		
	100E		42	50		42	50		48	58		

3

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D to Q	250	410	600	250	410	600	250	410	600		
	D to F	500	725	1000	500	725	100	500	725	1000		
t_{SKEW}	Within-Device Skew										ps	
	D to Q		75			75			75			1
t_r	Rise / Fall Times										ps	
t_f	20 - 80%											
	Q	275	450	700	275	450	700	275	450	700		
	F	300	475	700	300	475	700	300	475	700		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E111
MC100E111

1:9 DIFFERENTIAL CLOCK DRIVER

3

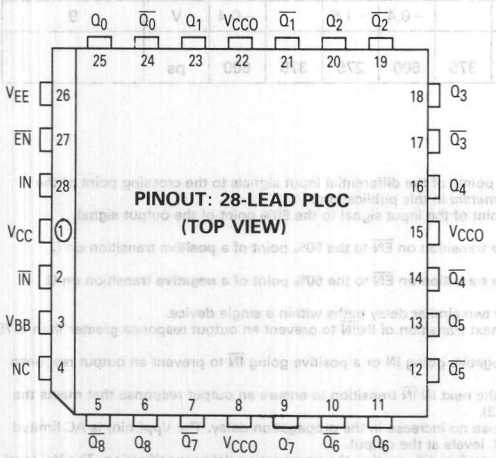
- Low Skew
- Guaranteed Skew Spec
- Differential Design
- V_{BB} Output
- Enable
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

The MC10E/100E111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

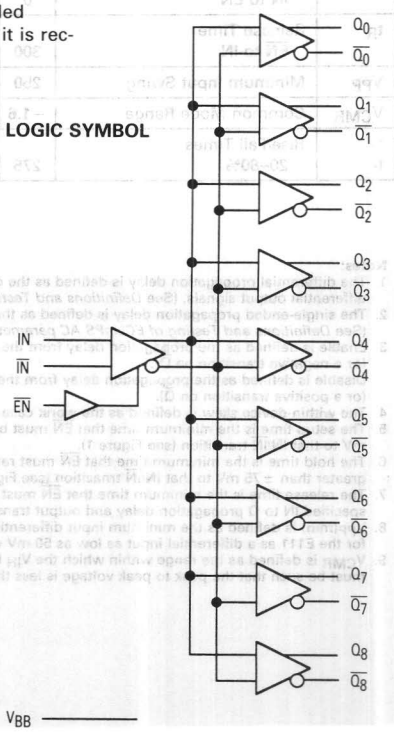
The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within-device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CCO}) as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 μF capacitor.



LOGIC SYMBOL



PIN NAMES

Pin	Function
IN, $\overline{IN}$	Differential Input Pair
$\overline{EN}$	Enable
Q_0, $\overline{Q_0}$–Q_8, $\overline{Q_8}$	Differential Outputs
V_{BB}	V_{BB} Output

AC CHARACTERISTICS: V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = 25°C			T_A = 85°C				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Note**
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	IN (differential)	430		630	430		630	430		630		1
	IN (single-ended)	330		730	330		730	330		730		2
	Enable	450		850	450		850	450		850		3
	Disable	450		850	450		850	450		850		3
t_{skew}	Within-Device Skew		25	50		25	50		25	50	ps	4
t_S	Setup Time $\overline{EN}$ to IN	200	0		200	0		200	0		ps	5
t_H	Hold Time IN to $\overline{EN}$	0	−200		0	−200		0	−200		ps	6
t_R	Release Time $\overline{EN}$ to IN	300	100		300	100		300	100		ps	7
V_{PP}	Minimum Input Swing	250			250			250			mV	8
V_{CMR}	Common Mode Range	−1.6		−0.4	−1.6		−0.4	−1.6		−0.4	V	9
t_r t_f	Rise/Fall Times 20–80%	275	375	600	275	375	600	275	375	600	ps	

Notes:
1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. (See *Definitions and Testing of ECLinPS AC Parameters* in this publication.)
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. (See *Definitions and Testing of ECLinPS AC parameters* in this publication.)
3. Enable is defined as the propagation delay from the 50% point of a **negative** transition on $\overline{EN}$ to the 50% point of a **positive** transition on Q (or a negative transition on $\overline{Q}$).
   Disable is defined as the propagation delay from the 50% point of a **positive** transition on $\overline{EN}$ to the 50% point of a **negative** transition on Q (or a positive transition on $\overline{Q}$).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition (see Figure 1).
6. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ trnasition (see Figure 2).
7. The release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.
9. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

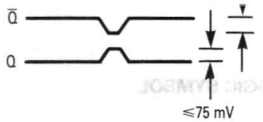


Figure 1

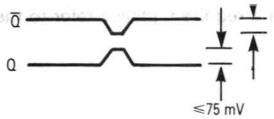


Figure 2

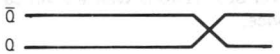


Figure 3

MC10E112
MC100E112

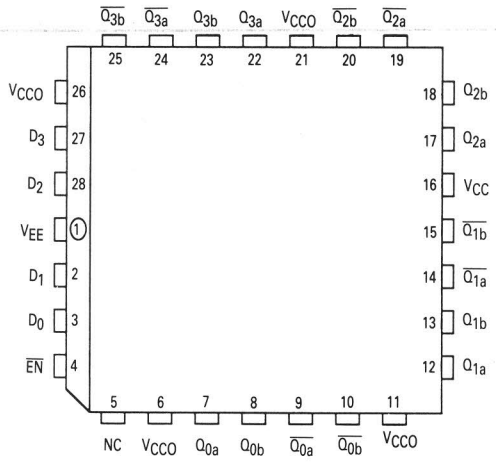
- 600 ps Max. Propagation Delay
- Common Enable Input
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

QUAD DRIVER

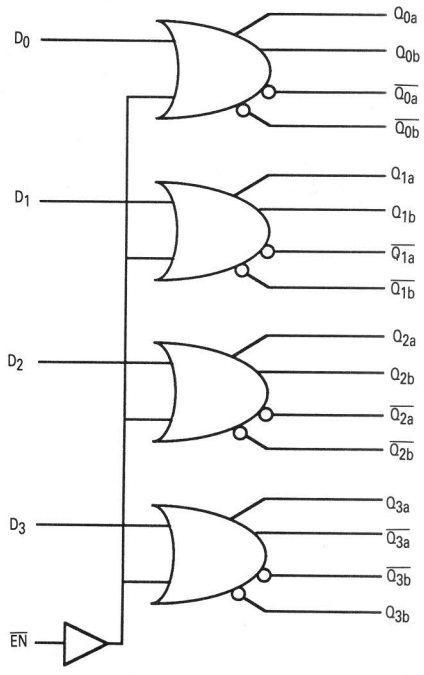
3

The MC10E/100E112 is a quad driver with two pairs of OR/NOR outputs from each gate, and a common, buffered enable input. Using the data inputs the device can serve as an ECL memory address fan-out driver. Using just the enable input, the device serves as a clock driver, although the MC10E/100E111 is designed specifically for this purpose, and offers lower skew than the E112. For memory address driver applications where scan capabilities are required, please refer to the E212 device.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0–D_3	Data Inputs
$\overline{EN}$	Enable Input
Q_{na}, Q_{nb}	True Outputs
$\overline{Q_{na}}$, $\overline{Q_{nb}}$	Inverting Outputs

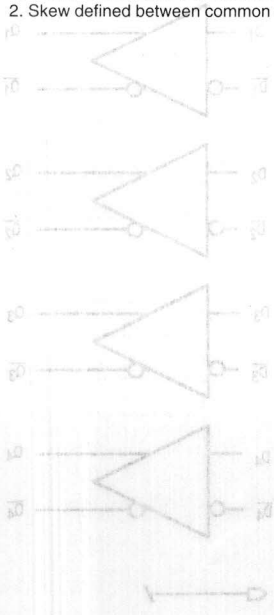
DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current										µA	
	D			200			200			200		
	$\overline{EN}$			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		47	56		47	56		47	56		
	100E		47	56		47	56		54	65		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	200	400	600	200	400	600	200	400	600		
	$\overline{EN}$	275	450	675	275	450	675	275	450	675		
t_{SKEW}	Within-Device Skew										ps	
	Dn to Qn, $\overline{Qn}$		80			80			80			1
	Qna to Qnb		40			40			40			2
t_r	Rise / Fall Times										ps	
t_f	20 - 80%	275	425	700	275	425	700	275	425	700		

1. Within-device skew is defined as identical transitions on similar paths through a device
2. Skew defined between common OR or common NOR outputs of a single gate.



inverting and non-inverting inputs are left open, in this case the Q output goes LOW, while the $\overline{Q}$ output goes HIGH. This feature makes the device ideal for twisted pair applications.

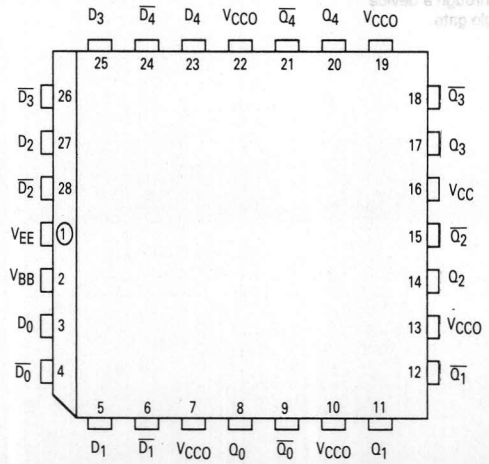
If both inverting and non-inverting inputs are at an equal potential of >–2.5 V, the receiver does *not* go to a defined state, but rather current-shares in normal differential amplifier fashion, producing output voltage levels midway between HIGH and LOW, or the device may even oscillate.

The device V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 μF capacitor. Please refer to the interface section of the design guide for information on using the E116 in specialized applications.

The E116 features input pull-down resistors, as does the rest of the ECLinPS family.

For application which require bandwidths greater than that of the E116, the E416 device may be of interest.

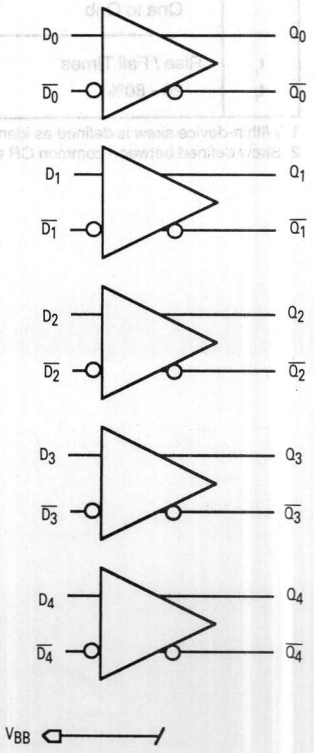
PINOUT: 28-LEAD PLCC (TOP VIEW)



PIN NAMES

Pin	Function
D_0, $\overline{D_0}$–D_4, $\overline{D_4}$	Differential Input Pairs
Q_0, $\overline{Q_0}$–Q_4, $\overline{Q_4}$	Differential Output Pairs
V_{BB}	Reference Voltage Output

LOGIC SYMBOL



DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
VBB	Output Reference Voltage										V	
	10E	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19		
	100E	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26		
I_{IH}	Input HIGH Current			200			200			200	µA	
I_{EE}	Power Supply Current										mA	
	10E		29	35		29	35		29	35		
	100E		29	35		29	35		33	40		
$V_{PP}(DC)$	Input Sensitivity	150			150			150			mV	1
VCMR	Common Mode Range	-2.0		-0.6	-2.0		-0.6	-2.0		-0.6	V	2

1. V_{PP} is the minimum differential input voltage required to assure full ECL levels are present at the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than V_{PPMIN} and < 1V.

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	200	300	450	200	300	450	200	300	450		
	D (SE)	150	300	500	150	300	500	150	300	500		
$V_{PP}(AC)$	Minimum Input Swing	150			150			150			mV	1
t_{SKEW}	Within-Device Skew										ps	
	Dn to Qn, $\overline{Qn}$		50			50			50			2
t_{SKEW}	Duty Cycle Skew											
	$t_{PLH} - t_{PHL}$		±10			±10			±10		ps	3
t_r	Rise / Fall Times										ps	
t_f	20 - 80%	275	375	575	275	375	575	275	375	575		

1. Minimum input swing for which AC parameters are guaranteed.
2. Within-device skew is defined as identical transitions on similar paths through a device
3. Duty cycle skew defined only for differential operation when the delays are measured from the cross point of the inputs to the cross points of the outputs

MC10E122
MC100E122

- 500 ps Max. Propagation Delay
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

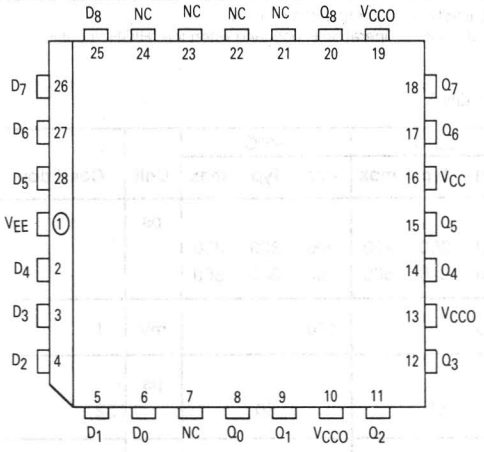
9-BIT BUFFER

3

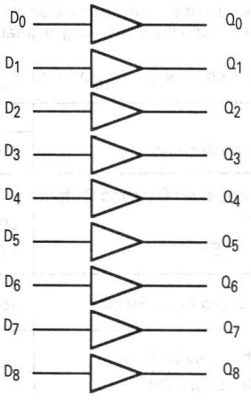
DESCRIPTION

The MC10E/100E122 is a 9-bit buffer. The device contains nine non-inverting buffer gates.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0–D_8	Data Inputs
Q_0–Q_8	Data Outputs

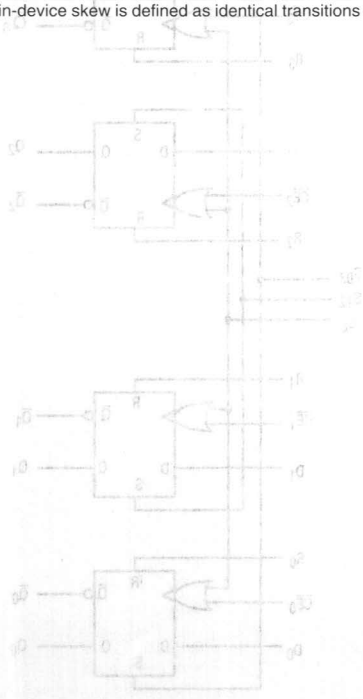
DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current			200			200			200	µA	
I_{EE}	Power Supply Current										mA	
	10E		41	49		41	49		41	49		
	100E		41	49		41	49		47	57		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	150	350	500	150	350	500	150	350	500	ps	
t_{SKEW}	Within-Device Skew D to Q		75			75			75		ps	1
t_r t_f	Rise / Fall Times 20 - 80%	300	425	800	300	425	800	300	425	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device

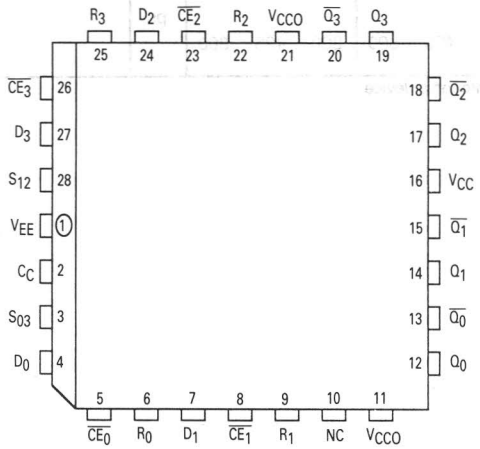


by holding the $\overline{CE}$ inputs LOW and using C_C to clock all four flip-flops. In this case, the $\overline{CE}$ inputs perform the function of controlling the common clock, to each flip-flop.

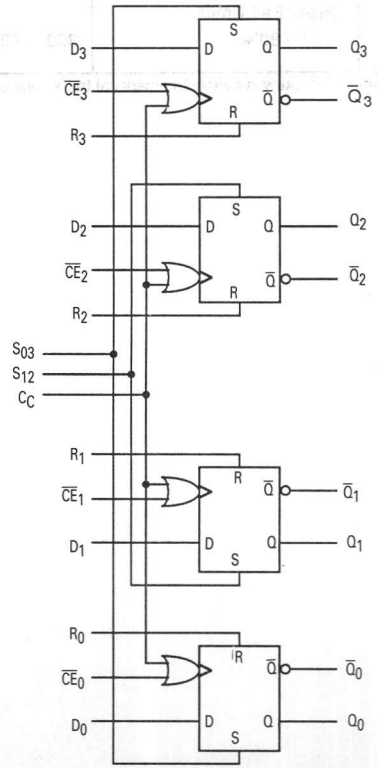
Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both C_C and $\overline{CE}$ are LOW, and transfers to the slave when either C_C or $\overline{CE}$ (or both) go HIGH.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0–D_3	Data Inputs
$\overline{CE}_0$–$\overline{CE}_3$	Clock Enables (Individual)
R_0–R_3	Resets
C_C	Common Clock
S_{03}, S_{12}	Sets (paired)
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Inverting Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current										µA	
	C_C			350			350			350		
	S			450			450			450		
	R			300			300			300		
	$\overline{CE}$			300			300			300		
	D			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		58	70		58	70		58	70		
	100E		58	70		58	70		67	81		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
f_{MAX}	Max. Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	$\overline{CE}$	360	500	700	360	500	700	360	500	700		
	CC	325	500	675	325	500	675	325	500	675		
	R	350	550	725	350	550	725	350	550	725		
	S	350	550	725	350	550	725	350	550	725		
t_s	Setup Time										ps	
	D	150	20		150	20		150	20			2
t_h	Hold Time										ps	
	D	175	-20		175	-20		150	-20			2
t_{RR}	Reset Recovery Time	400	150		400	150		400	150		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, S, R	400			400			400				
t_{SKEW}	Within-Device Skew		60			60			60		ps	1
t_r	Rise / Fall Times										ps	
t_f	20 - 80%	300	480	675	300	480	675	300	480	675		

1. Within-device skew is defined as identical transitions on similar paths through a device
2. Setup/hold times guaranteed for both C_C & $\overline{CE}$

MC10E136
MC100E136

6-BIT UNIVERSAL COUNTER

Product Preview

- 700MHz Min. Count Frequency
- Look-Ahead-Carry Input and Output
- Fully Synchronous Up and Down Counting
- Asynchronous Master Reset
- Internal 75kΩ Input Pulldown Resistors
- Extended 100E VEE Range of -4.2V to -5.46V

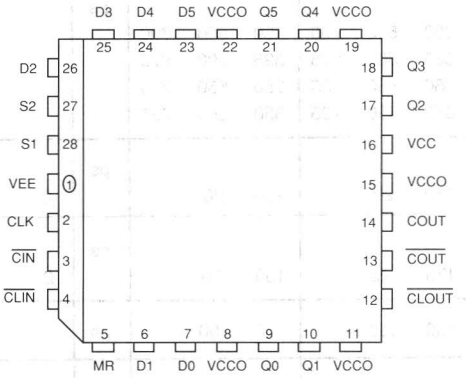
3

The MC 10E136/100E136 is an 6-bit synchronous, presettable, cascadable universal counter.

The device offers a look-ahead-carry input and generates a look-ahead-carry output. These two features allow for the cascading of multiple E136's to wider bit widths that operate at nearly the same frequency as a stand alone counter. The CLOUT output will pulse low for one clock cycle one count before the counter reaches terminal count.

The COUT pin will pulse low for one clock cycle when the counter reaches terminal count. The differential COUT output facilitates its use in programmable divider and self-stopping counter applications.

PINOUT: 28-LEAD PLCC (TOP VIEW)



PIN NAMES

PIN	FUNCTION
D0-D5	Preset Data Inputs
Q0-Q5	Differential Data Outputs
S1, S2	Mode Control Pins
MR	Master Reset
CLK	Clock Input
COUT,$\overline{\text{COUT}}$	Carry Out Output (Active LOW)
$\overline{\text{CLOUT}}$	Look-Ahead-Carry Output
$\overline{\text{CIN}}$	Carry In Input (Active LOW)
$\overline{\text{CLIN}}$	Look-Ahead-Carry Input

FUNCTION TABLE

S1	S2	$\overline{\text{CIN}}$	MR	CLK	Function
L	L	X	L	Z	Preset Parallel Data Inputs
L	H	L	L	Z	Increment (Count Up)
L	H	H	L	Z	Hold Count
H	L	L	L	Z	Decrement (Count Down)
H	L	H	L	Z	Hold Count
H	H	X	L	Z	Hold Count
X	X	X	H	X	Reset (Qn = LOW; COUT = HIGH)

Z = Low to High Transition

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Product Preview

MC10E137
MC100E137

8-BIT RIPPLE COUNTER

3

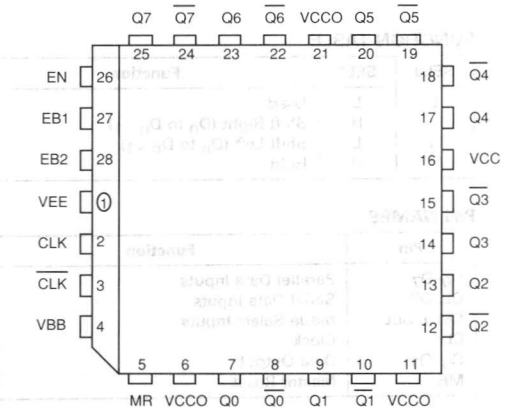
- 1.2GHz Min. Count Frequency
- Synchronous and Asynchronous Enable Pins
- Differential Clock Input and Data Output Pins
- Asynchronous Master Reset
- Internal 75kΩ Input Pulldown Resistors
- Extended 100E VEE Range of -4.2V to -5.46V

The MC10E/100E137 is a very high speed binary ripple counter. The two least significant bits were designed with very fast edge rates while the more significant bits maintain standard ECLinPS output edge rates. This allows the counter to operate at very high frequencies while maintaining a moderate power dissipation level.

Both synchronous and asynchronous enables are available to maximize the devices flexibility for various applications. The device is ideally suited for multiple frequency clock generation as well as a counter in a high performance ATE time measurement board.

The asynchronous Master Reset resets the counter to an all zero state upon assertion.

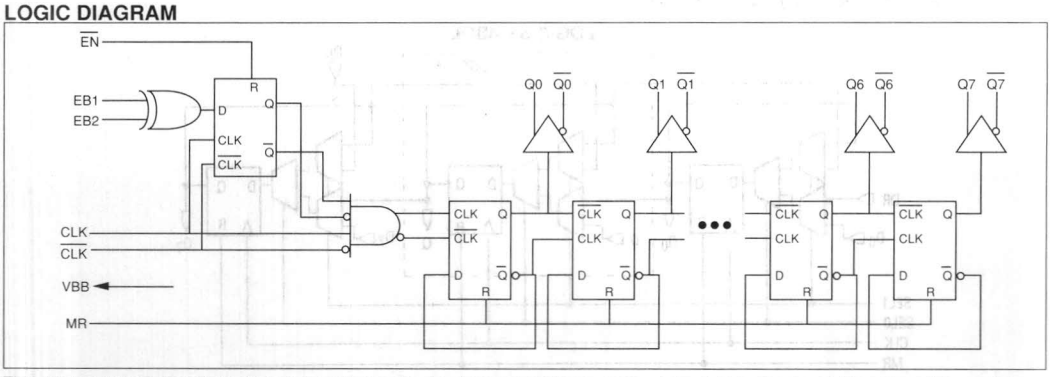
PINOUT: 28-LEAD PLCC (TOP VIEW)



PIN NAMES

PIN	FUNCTION
CLK, CLK	Differential Clock Inputs
Q0-Q7, Q0-Q7	Differential Q Outputs
EN	Asynchronous Enable Input
EB1, EB2	Synchronous Enable Inputs
MR	Asynchronous Master Reset
VBB	Switching Reference Output

LOGIC DIAGRAM

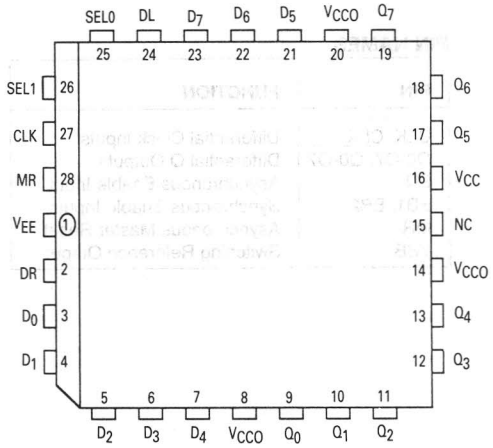


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

The select pins, SEL0 and SEL1, select one of four modes of operation: Load, Hold, Shift Left, Shift Right, according to the Function Table.

Input data is accepted a set-up time before the positive clock edge. A HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

PINOUT: 28-LEAD PLCC (TOP VIEW)



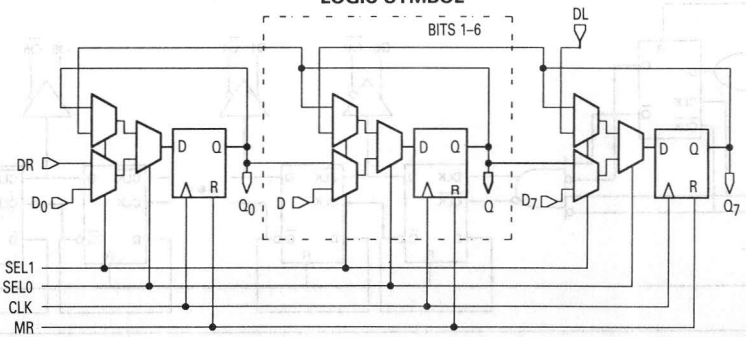
FUNCTION TABLE

SEL0	SEL1	Function
L	L	Load
L	H	Shift Right (D_n to D_{n+1})
H	L	Shift Left (D_n to D_{n-1})
H	H	Hold

PIN NAMES

Pin	Function
D_0–D_7	Parallel Data Inputs
DL, DR	Serial Data Inputs
SEL0, SEL1	Mode Select Inputs
CLK	Clock
Q_0–Q_7	Data Outputs
MR	Master Reset

LOGIC SYMBOL



DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		131	157		131	157		131	157		
	100E		131	157		131	157		151	181		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	Clk	625	750	975	625	750	975	625	750	975		
	MR	600	725	975	600	725	975	600	725	975		
t_s	Setup Time										ps	
	D	175	25		175	-125		175	+25			
	SEL0	350	200		350	+200		350	+200			
	SEL1	300	150		300	+150		300	+150			
t_h	Hold Time										ps	
	D	200	-25		200	-25		200	-25			
	SEL0	100	-200		100	-200		100	-200			
	SEL1	100	-150		100	-150		100	-150			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		60			60			60		ps	1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%	300	525	800	300	525	800	300	525	800		

1. Within-device skew is defined as identical transitions on similar paths through a device

EXPANDED FUNCTION TABLE

Function	DL	DR	SEL0	SEL1	MR	CLK	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Load	X	X	L	L	L	Z	D0	D1	D2	D3	D4	D5	D6	D7
Shift Right	X	L	L	H	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6
	X	H	L	H	L	Z	H	L	Q0	Q1	Q2	Q3	Q4	Q5
Shift Left	L	X	H	L	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	L
	H	X	H	L	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Hold	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

MC10E142
MC100E142

- 700 MHz Min. Shift Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

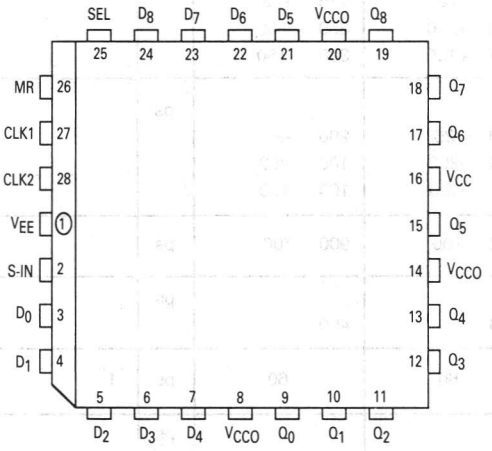
9-BIT SHIFT REGISTER

3

The MC10E/100E142 is a 9-bit shift register, designed with byte-parity applications in mind. The E142 performs serial/parallel in and serial/parallel out, shifting in one direction. The nine inputs D0–D8 accept parallel input data, while S-IN accepts serial input data.

The SEL (Select) input pin is used to switch between the two modes of operation — SHIFT and LOAD. The shift direction is from bit 0 to bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

PINOUT: 28-LEAD PLCC (TOP VIEW)



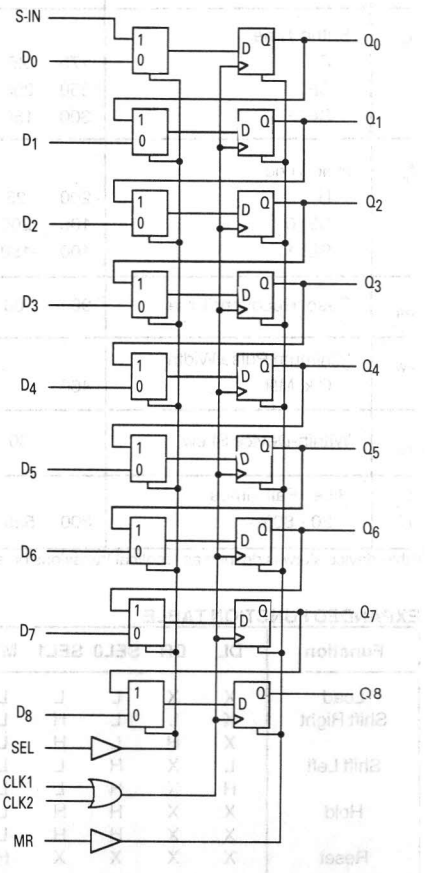
FUNCTION TABLE

SEL	Mode
L	LOAD
H	SHIFT

PIN NAMES

Pin	Function
D_0–D_8	Parallel Data Inputs
S-IN	Serial Data Input
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q_0–Q_8	Data Outputs

LOGIC SYMBOL



DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		120	145		120	145		120	145		
	100E		120	145		120	145		138	165		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	Clk	600	800	1000	600	800	1000	600	800	1000		
	MR	600	800	1000	600	800	1000	600	800	1000		
t_s	Setup Time										ps	
	D	50	-100		50	-100		50	-100			
	SEL	300	150		300	150		300	150			
t_h	Hold Time										ps	
	D	300	100		300	100		300	100			
	SEL	75	-150		75	-150		75	-150			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		75			75			75		ps	1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%	300	525	800	300	525	800	300	525	800		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E143
MC100E143

- 700 MHz Min. Operating Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

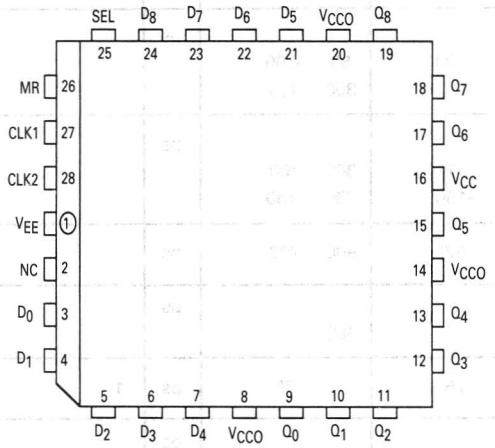
9-BIT HOLD REGISTER

3

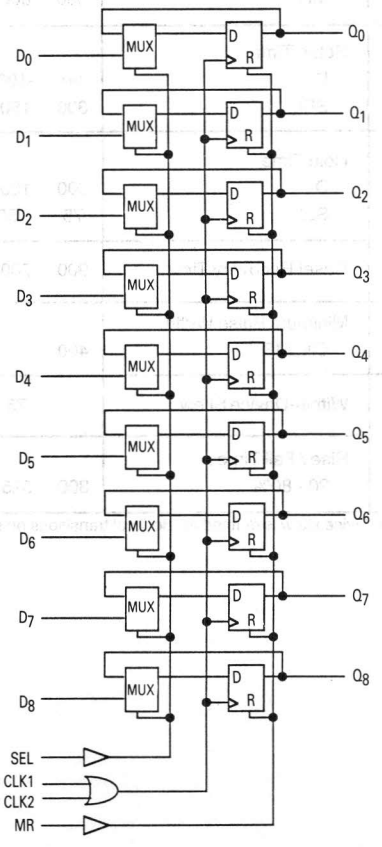
The MC10E/100E143 is a 9-bit holding register, designed with byte-parity applications in mind. The E143 holds current data or loads new data, with the nine inputs D0–D8 accepting parallel input data.

The SEL (Select) input pin is used to switch between the two modes of operation — HOLD and LOAD. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



FUNCTION TABLE

SEL	Mode
L	LOAD
H	HOLD

PIN NAMES

Pin	Function
D_0–D_8	Parallel Data Inputs
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q_0–Q_8	Data Outputs
NC	No Connection

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		120	145		120	145		120	145		
	100E		120	145		120	145		138	165		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
f_{MAX}	Max. Toggle Frequency	700	900		700	900		700	900		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	Clk	600	800	1000	600	800	1000	600	800	1000		
	MR	600	800	1000	600	800	1000	600	800	1000		
t_s	Setup Time										ps	
	D	50	-100		50	-100		50	-100			
	SEL	300	150		300	150		300	150			
t_h	Hold Time										ps	
	D	300	100		300	100		300	100			
	SEL	75	-150		75	-150		75	-150			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		75			75			75		ps	1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%	300	525	800	300	525	800	300	525	800		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E150
MC100E150

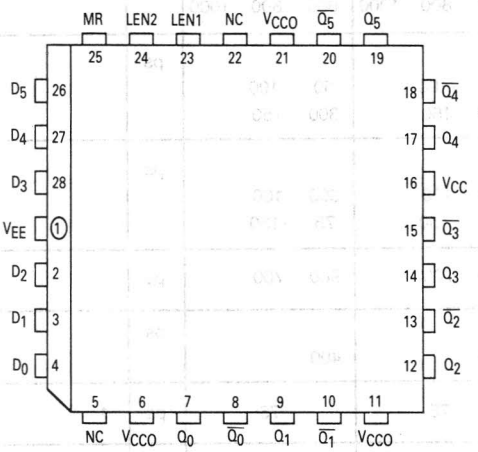
- 800 ps Max. Propagation Delay
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

6-BIT D LATCH

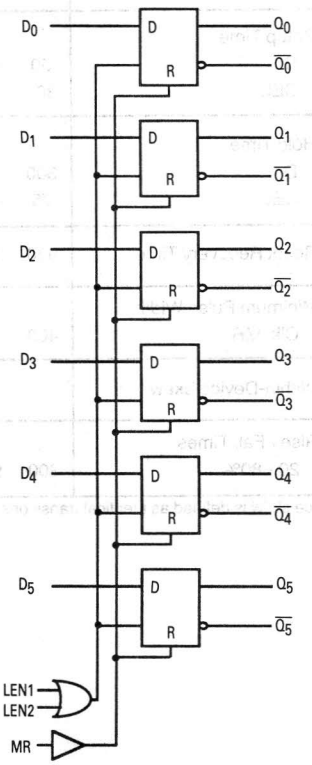
3

The MC10E/100E150 contains six D-type latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent and input data transitions propagate through to the output. A logic HIGH on either LEN1 or LEN2 (or both) latches the data. The Master Reset (MR) overrides all other controls to set the Q outputs low.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
LEN1, LEN2	Latch Enables
MR	Master Reset
Q_0–Q_5	True Outputs
$\overline{Q_0}$–$\overline{Q_5}$	Inverting Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current										µA	
	D			200			200			200		
	LEN, MR			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		52	62		52	62		52	62		
	100E		52	62		52	62		60	72		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	250	375	550	250	375	550	250	375	550		
	LEN	375	500	700	375	500	700	375	500	700		
	MR	450	625	750	450	625	750	350	625	750		
t_s	Setup Time										ps	
	D	200	50		200	50		200	50			
t_h	Hold Time										ps	
	D	200	-50		200	-50		200	-50			
t_{RR}	Reset Recovery Time	750	650		750	650		750	650			ps
t_{PW}	Minimum Pulse Width										ps	
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_r	Rise / Fall Times										ps	
t_f	20 - 80%	300	450	650	300	450	650	300	450	650		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E151
MC100E151

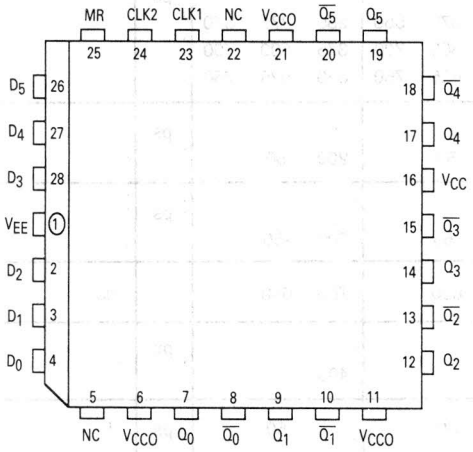
**6-BIT
D REGISTER**

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

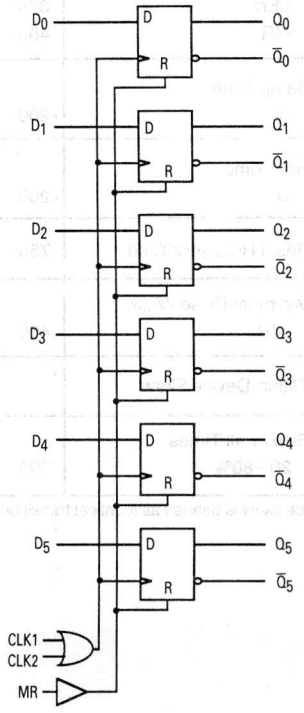
3

The MC10E/100E151 contains 6 D-type, edge-triggered, master-slave flip-flops with differential outputs. Data enters the master when both CLK1 and CLK2 are LOW, and is transferred to the slave when CLK1 or CLK2 (or both) go HIGH. The asynchronous Master Reset (MR) makes all Q outputs go LOW.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q_0–Q_5	True Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Inverted Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		65	78		65	78		65	78		
	100E		65	78		65	78		75	90		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
f_{MAX}	Max. Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	Clk	475	650	800	475	650	800	475	650	800		
	MR	475	650	850	475	650	850	475	650	850		
t_s	Setup Time										ps	
	D	0	-175		0	-175		0	-175			
t_h	Hold Time										ps	
	D	350	175		350	175		350	175			
t_{RR}	Reset Recovery Time	750	550		750	550		750	550			ps
t_{PW}	Minimum Pulse Width										ps	
	CLK, MR	400			400			400				
t_{SKEW}	Within-Device Skew		65			65			65		ps	1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%	300	450	700	300	450	700	300	450	700		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E154
MC100E154

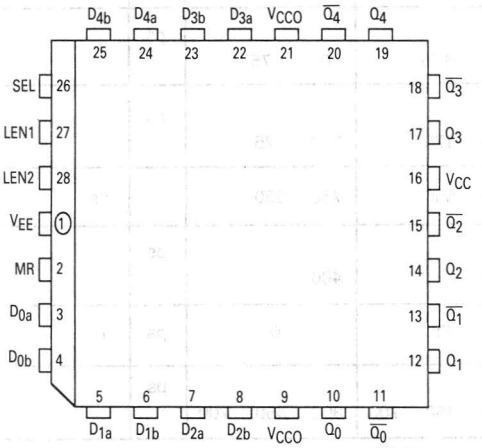
5-BIT
2:1 MUX-LATCH

- 850 ps Max. LEN to Output
- 825 ps Max. D to Output
- Differential Outputs
- Asynchronous Master Reset
- Dual Latch-Enables
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

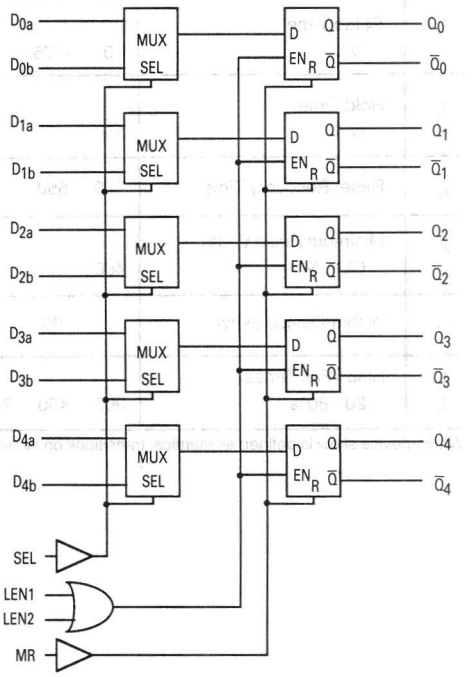
3

The MC10E/100E154 contains five 2:1 multiplexers followed by transparent latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output data is controlled by the multiplexer select control, SEL. A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_{0a}–D_{4a}	Input Data a
D_{0b}–D_{4b}	Input Data b
SEL	Data Select Input
LEN1, LEN2	Latch Enables
MR	Master Reset
Q_0–Q_4	True Outputs
$\overline{Q_0}$–$\overline{Q_4}$	Inverted Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		76	91		76	91		76	91		
	100E		76	91		76	91		87	105		

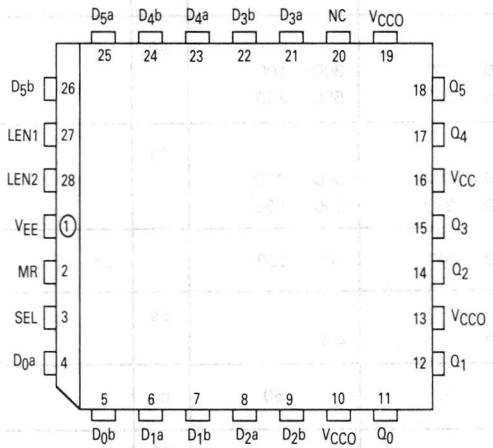
AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	D	325	500	700	325	500	700	325	500	700		
	SEL	475	650	925	475	650	925	475	650	925		
	LEN	350	500	750	350	500	750	350	500	750		
	MR	450	600	800	450	600	800	450	600	800		
t_s	Setup Time										ps	
	D	300	100		300	100		300	100			
	SEL	500	250		500	250		500	250			
t_h	Hold Time										ps	
	D	300	-100		300	-100		300	-100			
	SEL	200	-250		200	-250		200	-250			
t_{RR}	Reset Recovery Time	800	600		800	600		800	600			ps
t_{PW}	Minimum Pulse Width										ps	
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%	300	475	800	300	475	800	300	475	800		

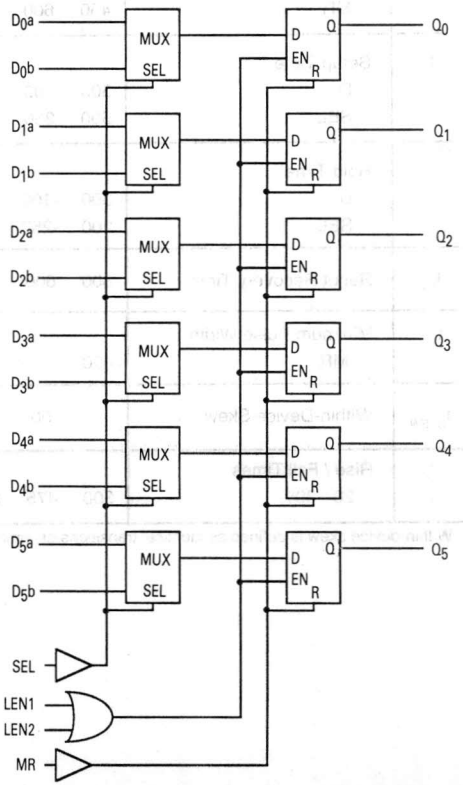
1. Within-device skew is defined as identical transitions on similar paths through a device

LOW, the latch is transparent, and output data is controlled by the multiplexer select control, SEL. A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0a–D_4a	Input Data a
D_0b–D_4b	Input Data b
SEL	Data Select Input
LEN1, LEN2	Latch Enables
MR	Master Reset
Q_0–Q_4	Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		85	102		85	102		85	102		
	100E		85	102		85	102		98	117		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	D	325	500	700	325	500	700	325	500	700		
	SEL	475	675	925	475	675	925	475	675	925		
	LEN	350	500	750	350	500	750	350	500	750		
	MR	450	600	850	450	600	850	450	600	850		
t_s	Setup Time										ps	
	D	300	100		300	100		300	100			
	SEL	500	250		500	250		500	250			
t_h	Hold Time										ps	
	D	300	-100		300	-100		300	-100			
	SEL	0	-250		0	-250		0	-250			
t_{RR}	Reset Recovery Time	800	650		800	650		800	650		ps	
t_{PW}	Minimum Pulse Width										ps	
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		75			75			75		ps	1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%	300	450	800	300	450	800	300	450	800		

1. Within-device skew is defined as identical transitions on similar paths through a device

3

MC10E156
MC100E156

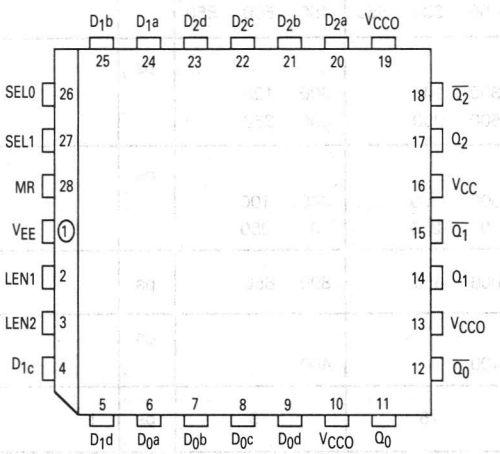
**3-BIT
4:1 MUX-LATCH**

- 950 ps Max. D to Output
- 850 ps Max. LEN to Output
- Differential Outputs
- Asynchronous Master Reset
- Dual Latch-Enables
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

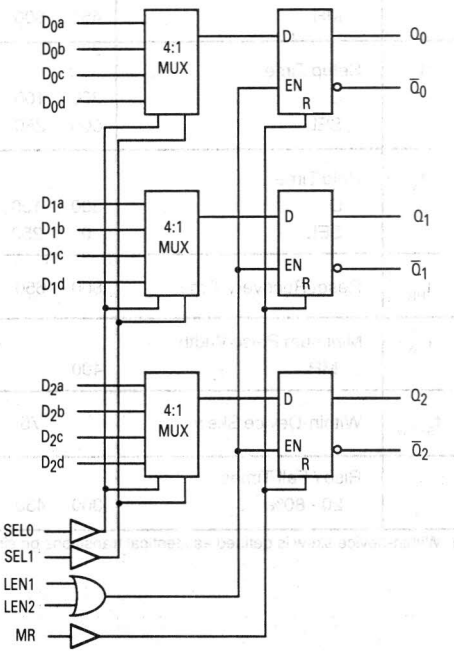
3

The MC10E/100E156 contains three 4:1 multiplexers followed by transparent latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output data is controlled by the multiplexer select controls (SEL0, SEL1). A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0x–D_3x	Input Data
SEL0, SEL1	Select Inputs
LEN1, LEN2	Latch Enables
MR	Master Reset
Q_0–Q_2	True Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Inverted Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		75	90		75	90		75	90		
	100E		75	90		75	90		86	103		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	D	400	600	900	400	600	900	400	600	900		
	SEL0	550	775	1050	550	775	1050	550	775	1050		
	SEL1	450	650	900	450	650	900	450	650	900		
	LEN	350	500	800	350	500	800	350	500	900		
	MR	350	600	825	350	600	825	350	600	825		
t_s	Setup Time										ps	
	D	400	275		400	275		400	275			
	SEL0	700	300		700	300		700	300			
	SEL1	600	400		600	400		600	400			
t_h	Hold Time										ps	
	D	300	-275		300	-275		300	-275			
	SEL0	100	-300		100	-300		100	-300			
	SEL1	200	-400		200	-400		200	-400			
t_{RR}	Reset Recovery Time	800	600		800	600		800	600			ps
t_{PW}	Minimum Pulse Width										ps	
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%	275	475	700	275	475	700	275	475	700		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E157
MC100E157

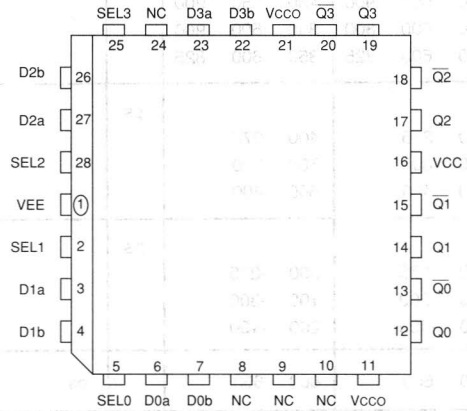
QUAD
2:1 MULTIPLEXER

- Individual Select Controls
- 550 ps Max. D to Output
- 800 ps Max. SEL to Output
- Extended 100E VEE Range of -4.2V to -5.46V
- Internal 75kΩ Input Pulldown Resistors

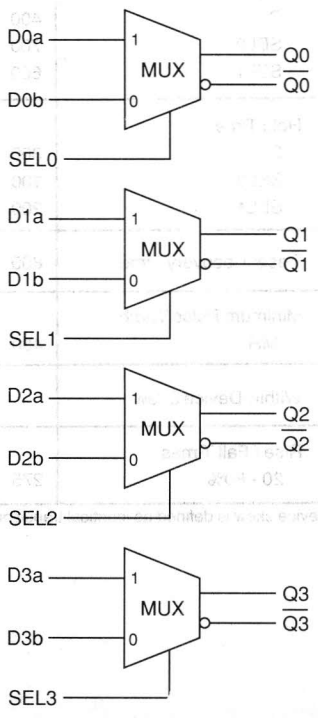
The MC 10E/100E157 contains four 2:1 multiplexers with differential outputs. The ouput data are controlled by the individual Select (SEL) inputs. The individual select control makes the devices well suited for random logic designs.

3

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



FUNCTION TABLE

SEL	Data
H	a
L	b

PIN NAMES

PIN	FUNCTION
D0a – D3a	Input Data a
D0b – D3b	Input Data b
SEL0 – SEL3	Select Inputs
Q0 – Q3	True Outputs
$\overline{Q0}$ – $\overline{Q3}$	Inverted Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current										µA	
	D			200			200			200		
	SEL			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		32	38		32	38		32	38		
	100E		32	38		32	38		37	44		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	220	380	550	220	380	550	220	380	550		
	SEL	425	600	800	425	600	800	425	600	800		
t_{SKEW}	Within-Device Skew		70			70			70		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	400	650	275	400	650	275	400	650		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E158
MC100E158

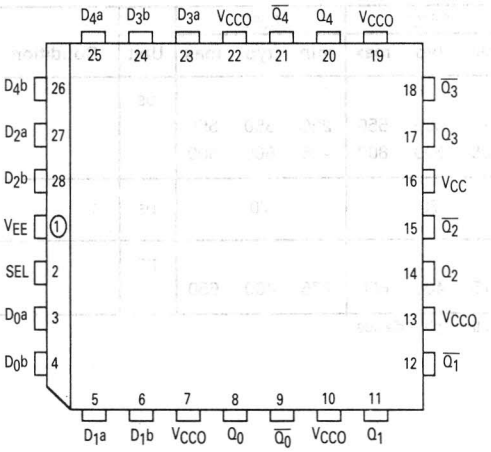
- 600 ps Max. D to Output
- 800 ps Max. SEL to Output
- Differential Outputs
- One V_{CCO} Pin Per Output Pair
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

5-BIT
2:1 MULTIPLEXER

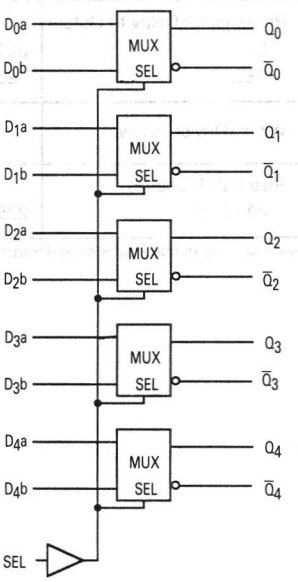
3

The MC10E/100E158 contains five 2:1 multiplexers with differential outputs. The output data are controlled by the Select input (SEL).

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



FUNCTION TABLE

SEL	Data
H	a
L	b

PIN NAMES

Pin	Function
D_0a–D_4a	Input Data a
D_0b–D_4b	Input Data b
SEL	Select Input
Q_0–Q_4	True Outputs
$\overline{Q_0}$–$\overline{Q_4}$	Inverted Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current										µA	
	D			200			200			200		
	SEL			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		33	40		33	40		33	40		
	100E		33	40		33	40		38	46		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	225	385	550	225	385	550	225	385	550		
	SEL	400	600	775	400	600	775	400	600	775		
t_{SKEW}	Within-Device Skew		60			60			60		ps	1
t_r	Rise / Fall Time										ps	
t_f	20 - 80%	275	425	650	275	425	650	275	425	650		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E160
MC100E160

12-BIT PARITY GENERATOR/CHECKER

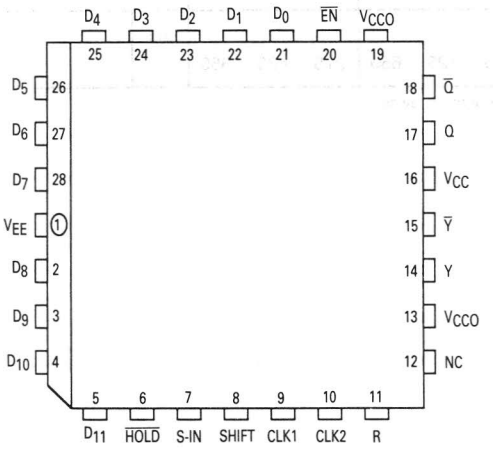
- Provides Odd-HIGH Parity of 12 Inputs
- Shiftable Output Register with Hold
- 900 ps Max. D to Q/$\overline{Q}$ Output
- Enable
- Asynchronous Register Reset
- Dual Clocks
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

3

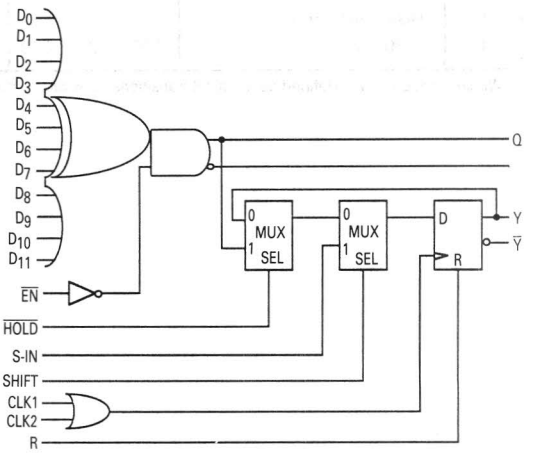
The MC10E/100E160 is a 12-bit parity generator/checker. The Q output is HIGH when an odd number of inputs are HIGH. A HIGH on the Enable input ($\overline{EN}$) forces the Q output LOW.

The E160 also features an output register. Multiplexers direct the register input, giving the option of holding present data by asserting $\overline{HOLD}$ LOW, or of shifting data in through the S-IN pin by asserting SHIFT HIGH. The output register itself is clocked by a positive edge on CLK1 or CLK2 (or both). A HIGH on the reset pin (R) overrides to force the Y output LOW.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0–D_{11}	Data Inputs
S-IN	Serial Data Input
$\overline{EN}$	Enable, active LOW
$\overline{HOLD}$	Hold, active LOW
SHIFT	Shift, active HIGH
CLK1, CLK2	Clock Inputs
R	Reset Input
Q, $\overline{Q}$	Direct Output
Y, $\overline{Y}$	Register Output

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH} / t_{PHL}	Propagation Delay to Output										ps	
	D to Q	400	650	950	400	650	950	400	650	950		
	$\overline{EN}$ to Q	300	550	750	300	550	750	300	550	750		
	CLK to Y	275	500	700	275	500	700	275	500	700		
	R to Y	275	500	725	275	500	725	275	500	725		
t_s	Setup Time										ps	
	D	1200	900		1200	900		1200	900			
	$\overline{HOLD}$	600	300		600	300		600	300			
	S-IN	350	150		350	150		350	150			
	SHIFT	500	250		500	250		500	250			
t_h	Hold Time										ps	
	D	-400	-900		-400	-900		-400	-900			
	$\overline{HOLD}$	100	-300		100	-300		100	-300			
	S-IN	300	-150		300	-150		300	-150			
	SHIFT	200	-250		200	-250		200	-250			
t_r / t_f	Rise / Fall Time										ps	
	20 - 80%	300	450	650	300	450	650	300	450	650		

1. Within a device skew is guaranteed for identical transitions on similar paths through a device

MC10E163
MC100E163

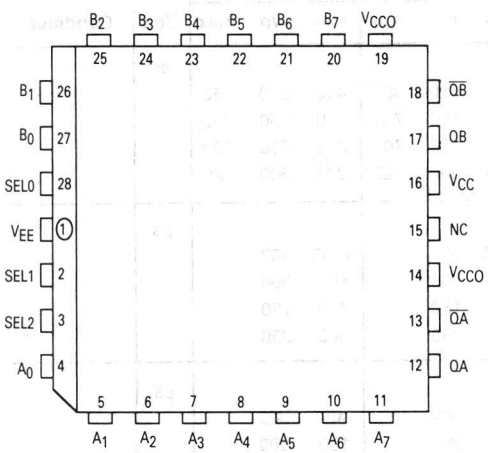
- 850 ps Max. D to Output
- Differential Outputs
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

2-BIT
8:1 MULTIPLEXER

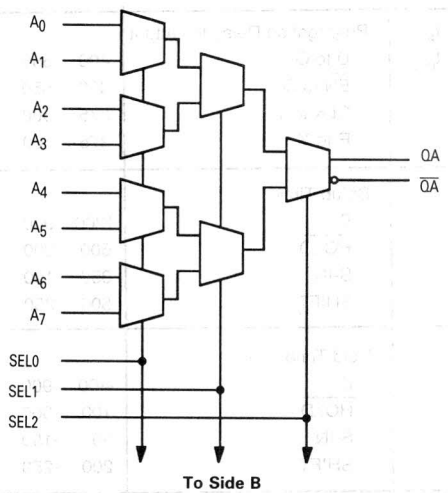
3

The MC10E/100E163 contains two 8:1 multiplexers with differential outputs and common select inputs. The select inputs (SEL0, 1, 2) control which one of the eight data inputs (A_0–A_7, B_0–B_7) is propagated to the output.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



FUNCTION TABLE

SEL2	SEL1	SEL0	A/B Data
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

PIN NAMES

Pin	Function
A_0–A_7	A Data Inputs
B_0–B_7	B Data Inputs
SEL0, 1, 2	Select Inputs
QA, QB	True Outputs
$\overline{QA}$, $\overline{QB}$	Inverting Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

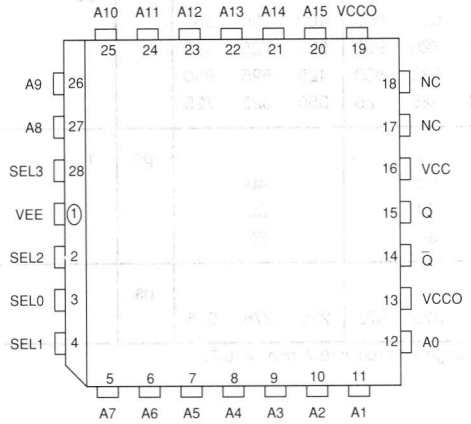
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		73	88		73	88		73	88		
	100E		73	88		73	88		83	100		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

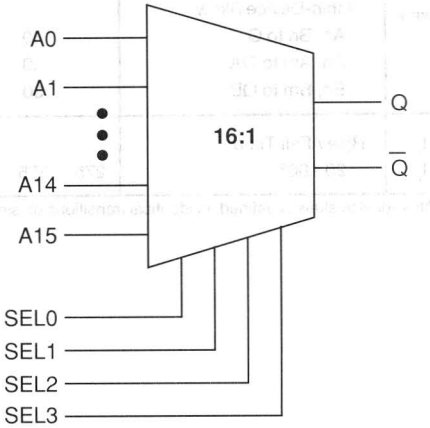
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output											ps
t_{PHL}	D	400	550	800	400	550	800	400	550	800		
	SEL0	525	725	950	525	725	950	525	725	950		
	SEL1	425	625	850	425	625	850	425	625	850		
	SEL2	350	525	725	350	525	725	350	525	725		
t_{SKEW}	Within-Device Skew										ps	1
	An, Bn to Q		40			40			40			
	An, Am to QA		30			30			30			
	Bn, Bm to QB		30			30			30			
t_r	Rise / Fall Time										ps	
t_f	20 - 80%	275	375	575	275	375	575	275	375	575		

1. Within-device skew is defined as identical transitions on similar paths through a device; n=0-7, m n, m=0-7.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

PIN	FUNCTION
A0 – A15	Data Inputs
SEL[0:3]	Select Inputs
Q, $\overline{Q}$	Output

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		59	71		59	71		59	71		
	100E		59	71		59	71		68	81		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	A Input	350	600	850	350	600	850	350	600	850		
	SEL0	500	700	900	500	700	900	500	700	900		
	SEL1	400	675	900	400	675	900	400	675	900		
	SEL2	400	675	900	400	675	900	400	675	900		
	SEL3	400	550	700	400	550	700	400	550	700		
t_{SKEW}	Within Device Skew		50			50			50		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	400	550	275	400	550	275	400	550		

1 Within Device skew is defined as the difference in the A to Q delay between the 16 different A inputs.

FUNCTION TABLE

SEL3	SEL2	SEL1	SEL0	Data
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	L	L	L	A8
H	L	L	H	A9
H	L	H	L	A10
H	L	H	H	A11
H	H	L	L	A12
H	H	L	H	A13
H	H	H	L	A14
H	H	H	H	A15

MC10E166
MC100E166

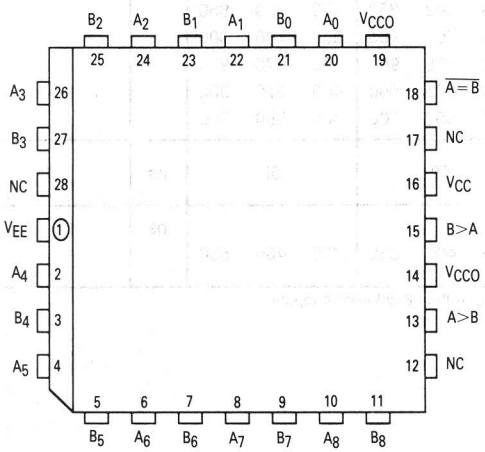
- 1100 ps Max. $\overline{A=B}$
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

9-BIT MAGNITUDE COMPARATOR

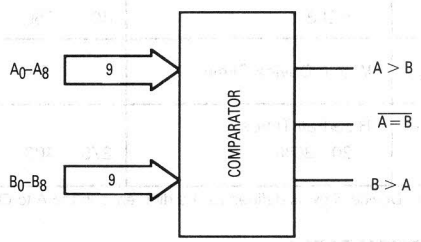
The MC10E/100E166 is a 9-bit magnitude comparator which compares the binary value of two 9-bit words and indicates whether one word is greater than, or equal to, the other.

3

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
A_0–A_8	A Data Inputs
B_0–B_8	B Data Inputs
A > B	A Greater than B Output
B > A	B Greater than A Output
$\overline{A=B}$	A Equal to B Output (active-LOW)

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		113	136		113	136		113	136		
	100E		113	136		113	136		130	156		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D to A=B	500	750	1100	500	750	1100	500	750	1100		
	D to A<B, A>B	500	850	1400	500	850	1400	500	850	1400		
t_r	Rise / Fall Time										ps	
t_f	20 - 80%	300	450	800	300	450	800	300	450	800		

MC10E167
MC100E167

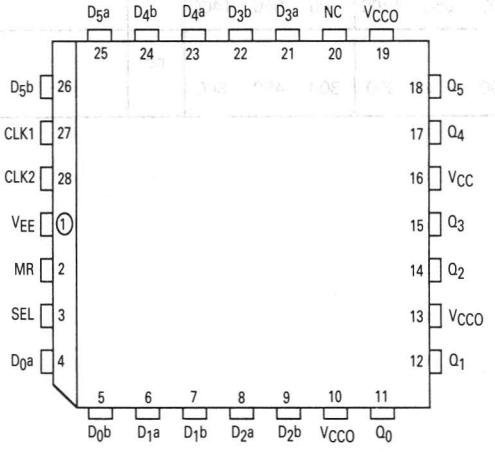
6-BIT
2:1 MUX-REGISTER

- 1000 MHz Min. Operating Frequency
- 800 ps Max. Clock to Output
- Single-Ended Outputs
- Asynchronous Master Resets
- Dual Clocks
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

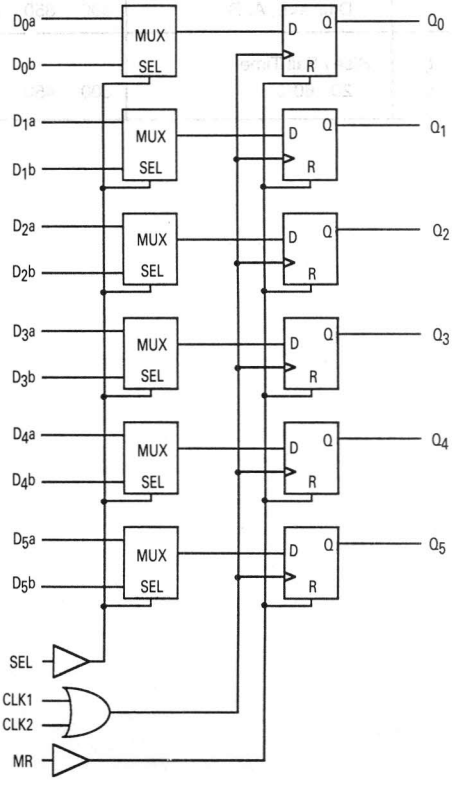
3

The MC10E/100E167 contains six 2:1 multiplexers followed by D flip-flops with single-ended outputs. Input data are selected by the Select control, SEL. The selected data are transferred to the flip-flop outputs by a positive edge on CLK1 or CLK2 (or both). A HIGH on the Master Reset (MR) pin asynchronously forces all Q outputs LOW.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



FUNCTION TABLE

SEL	Data
H	a
L	b

PIN NAMES

Pin	Function
D_0a–D_5a	Input Data a
D_0b–D_5b	Input Data b
SEL	Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q_0–Q_5	Data Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		94	113		94	113		94	113		
	100E		94	113		94	113		108	130		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
f_{MAX}	Max. Toggle Frequency	1000	1400		1000	1400		1000	1400		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	Clk	450	650	800	450	650	800	450	650	800		
	MR	450	650	850	450	650	850	450	650	850		
t_s	Setup Time										ps	
	D	100	-50		100	-50		100	-50			
	SEL	275	125		275	125		275	125			
t_h	Hold Time										ps	
	D	300	50		300	50		300	50			
	SEL	75	-125		75	-125		75	-125			
t_{RR}	Reset Recovery Time	750	550		750	550		750	550		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		75			75			75		ps	1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%	300	450	800	300	450	800	300	450	800		

1. Within-device skew is defined as identical transitions on similar paths through a device

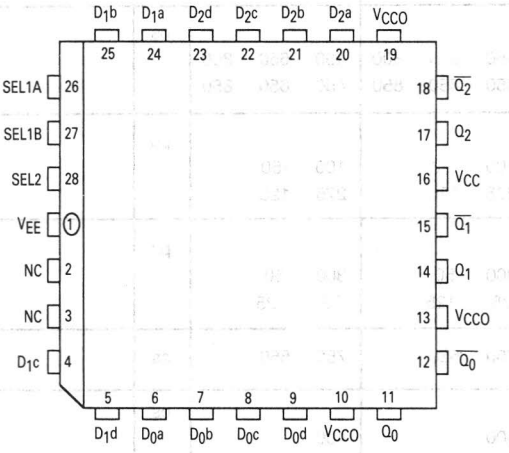
MC10E171
MC100E171

**3-BIT
4:1 MULTIPLEXER**

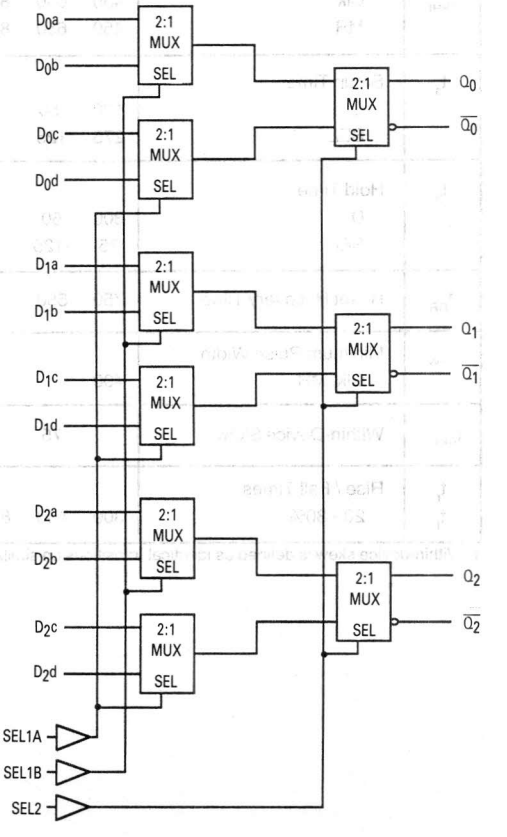
- 725 ps Max. D to Output
- Split Select
- Differential Outputs
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

The MC10E/100E171 contains three 4:1 multiplexers with differential outputs. Separate Select controls are provided for the leading 2:1 mux pairs (see logic symbol). The three Select inputs control which one of the four data inputs in each case is propagated to the corresponding output.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



FUNCTION TABLE

Pin	State	Operation
SEL2	H	Output c/d data
SEL1A	H	Input d data
SEL1B	H	Input b data

PIN NAMES

Pin	Function
D_0x–D_2x	Data Inputs
SEL1A, SEL1B	First-stage Select Inputs
SEL2	Second-stage Select Input
Q_0–Q_2	True Output
$\overline{Q_0}$–$\overline{Q_2}$	Inverted Output

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		56	67		56	67		56	67		
	100E		56	67		56	67		65	77		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

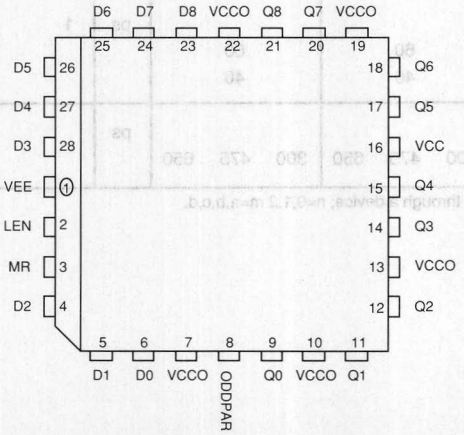
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	275	480	650	275	480	650	275	480	650		
	SEL1	450	650	850	450	650	850	450	650	850		
	SEL2	350	550	700	350	550	700	350	550	700		
t_{SKEW}	Within-Device Skew										ps	1
	Dnm, Dnm to Qn		60			60			60			
	Da, Db, Dc, Dd to Q		40			40			40			
t_r	Rise / Fall Time										ps	
t_f	20 - 80%	300	475	650	300	475	650	300	475	650		

1. Within-device skew is defined as identical transitions on similar paths through a device; n=0,1,2 m=a,b,c,d.

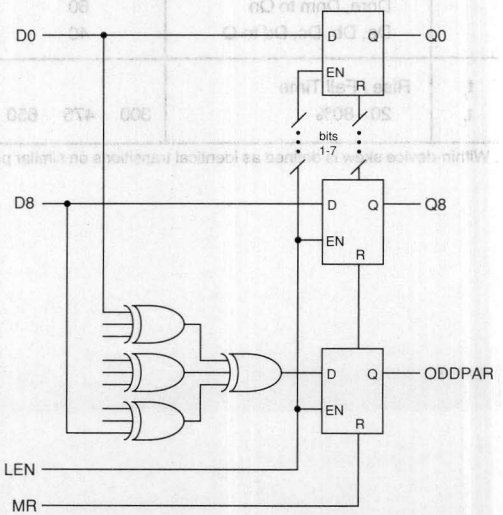
select (L = even parity, H = odd parity), and using ODDPAR as the byte parity output.

The LEN pin latches the data when asserted with a logical high and makes the latch transparent when placed at a logic low level.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

PIN	FUNCTION
D0 – D8	Data Inputs
LEN	Latch Enable
MR	Master Reset
Q0 – Q8	Data Outputs
ODDPAR	Parity Output

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		110	132		110	132		110	132		
	100E		110	132		110	132		127	152		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	D to Q	450	600	800	450	600	800	450	600	800		
	D to ODDPAR	850	1150	1450	850	1150	1450	850	1150	1450		
	LEN to Q	525	700	900	525	700	900	525	700	900		
	LEN to ODDPAR	525	700	900	525	700	900	525	700	900		
	MR to Q (t_{PHL})	525	700	900	525	700	900	525	700	900		
	MR to ODDPAR (t_{PHL})	525	700	900	525	700	900	525	700	900		
t_s	Setup Time										ps	
	D (Q)	275	100		275			275				
	D (ODDPAR)	900	700		900			900				
t_h	Hold Time										ps	
	D (Q)	175	-100		175			175				
	D (ODDPAR)	-300	-700		-300			-300				
t_{RR}	Reset Recovery Time	850	600		850	600		850	600		ps	
t_{SKEW}	Within-Device Skew										ps	1
	LEN, MR		75			75			75			
	D to Q		75			75			75			
	D to ODDPAR		200			200			200			
t_r t_f	Rise/Fall Times										ps	
	20 - 80%	300	500	800	300	500	800	300	500	800		

1. Within-device skew is defined as identical transitions on similar paths through a device

FUNCTION TABLE

D	EN	MR	Q	ODDPAR
H	L	L	H	H if odd no. of Dn HIGH
L	L	L	L	H if odd no. of Dn HIGH
X	H	L	Q_0	Q_0
X	X	H	L	L

MC10E193
MC100E193

- Hamming Code Generation
- 8-Bit Word, Expandable
- Provides Parity of Whole Word
- Scannable Parity Register
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

ERROR DETECTION/ CORRECTION CIRCUIT

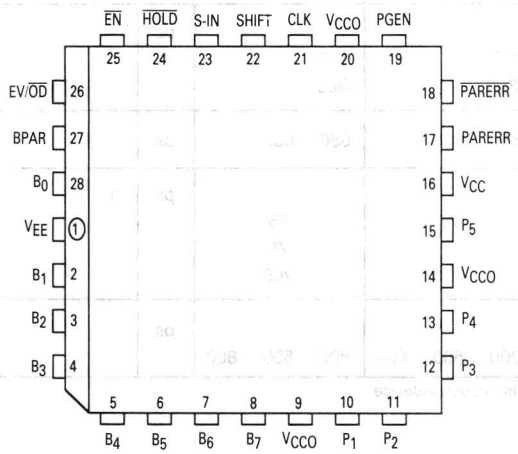
3

The MC10E/100E193 is an error detection and correction (EDAC) circuit. Modified Hamming parity codes are generated on an 8-bit word according to the pattern shown in the logic symbol. The P5 output gives the parity of the whole word. The word parity is also provided at the PGEN pin, after Odd/Even parity control and gating with the BPAR input. This output also feeds to a 1-bit shiftable register, for use as part of a scan ring.

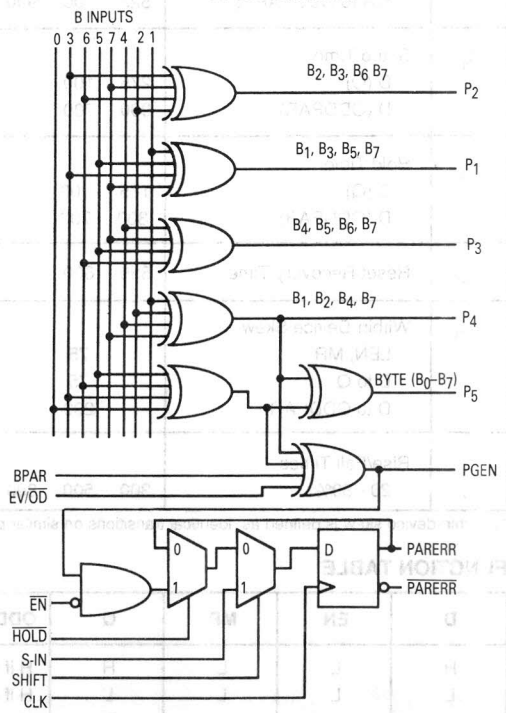
The combinatorial part of the device generates the same code pattern as the MC10193, a member of the MECL 10K family. The user is referred to the 10193 data sheet in the *MECL Device Data Book* for a fuller description of pattern expansion to long words, along with check bit generation and decoding schemes.

Used in conjunction with 12-bit parity generators such as the E160, a SECDED (single error correction, double error detection) error system can be designed for a multiple of an 8-bit word.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		112	134		112	134		112	134		
	100E		112	134		112	134		129	155		

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	B to P1, P2, P3, P4	350	700	1000	350	700	1000	350	700	1000		
	B to P5	400	775	1150	400	775	1150	400	775	1150		
	EV/$\overline{OD}$, BPAR to PGEN	350	650	850	350	650	850	350	650	850		
	B to PGEN	600	1000	1450	600	1000	1450	600	1000	1450		
	CLK to PARERR	300	550	850	300	550	850	300	550	850		
t_s	Setup Time										ps	
	SHIFT	400	150		400	150		400	150			
	$\overline{S\text{-}IN}$	300	50		300	50		300	50			
	$\overline{HOLD}$	750	350		750	350		750	350			
	$\overline{EN}$	500	250		500	250		500	250			
	EV/$\overline{OD}$	1300	850		1300	850		1300	850			
	BPAR	1300	850		1300	850		1300	850			
	B	1700	1100		1700	1100		1700	1100			
t_h	Hold Time										ps	
	SHIFT	200	-150		200	-150		200	-150			
	$\overline{S\text{-}IN}$	300	-50		300	-50		300	-50			
	$\overline{HOLD}$	100	-350		100	-350		100	-350			
	$\overline{EN}$	100	-250		100	-250		100	-250			
	EV/$\overline{OD}$	-200	-850		-200	-850		-200	-850			
	BPAR	-200	-850		-200	-850		-200	-850			
	B	-300	-1100		-300	-1100		-300	-1100			
t_r	Rise / Fall Times										ps	
t_f	20 - 80%	300	700	1100	300	7000	1100	300	700	1100		

3

by the seven address inputs D[0:6], which are latched on chip by a high signal on the latch enable (LEN) control.

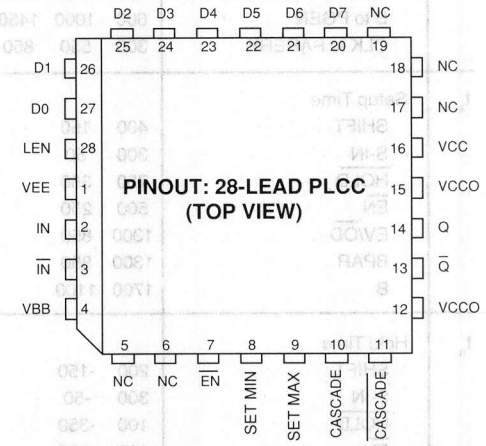
Because the delay programmability of the E195 is achieved by purely differential ECL gate delays the device will operate at frequencies of >1GHz while maintaining over 600mV of output swing.

The E195 thus offers very fine resolution, at very high frequencies, that is selectable entirely from a digital input allowing for very accurate system clock timing.

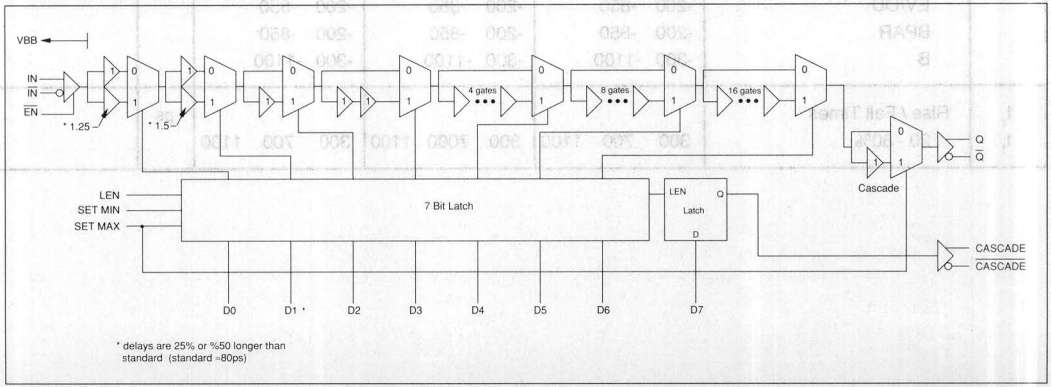
PIN NAMES

Pin	Function
IN/$\overline{IN}$	Signal Input
$\overline{EN}$	Input Enable
D[0:7]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Min Delay Set
SET MAX	Max Delay Set
CASCADE	Cascade Signal

logic allows full control of multiple PDC's, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.



LOGIC DIAGRAM - SIMPLIFIED



DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		130	156		130	156		130	156		
	100E		130	156		130	156		150	179		

3

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay										ps	
t_{PHL}	IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765		
	$\overline{IN}$ to Q; Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720		
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950		
	D7 to CASCADE	300	450	700	300	450	700	300	450	700		
t_{RANGE}	Programmable Range											
	t_{PD} (max) - t_{PD} (min)	2000	2175		2050	2240		2375	2580		ps	
Δt	Step Delay										ps	6
	D0 High		17			17.5			21			
	D1 High		34			35			42			
	D2 High	55	68	105	55	70	105	65	84	120		
	D3 High	115	136	180	115	140	180	140	168	205		
	D4 High	250	272	325	250	280	325	305	336	380		
	D5 High	505	544	620	515	560	620	620	672	740		
	D6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450		
Lin	Linearity	D1	D0		D1	D0		D1	D0			7
t_{SKEW}	Duty Cycle Skew											
	t_{PHL} - t_{PLH}		±30			±30			±30		ps	1
t_s	Setup Time										ps	
	D to LEN	200	0		200	0		200	0			
	D to IN	800			800			800				2
	$\overline{EN}$ to IN	200			200			200				3
t_h	Hold Time										ps	
	LEN to D	500	250		500	250		500	250			
	IN to $\overline{EN}$	0			0			0				4

AC Characteristics (Cont): $V_{EE} = V_{EE}$(min) to V_{EE}(max); $V_{CC} = V_{CCO}$ = GND

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		min	typ	max	min	typ	max	min	typ	max		
t_R	Release Time										ps	
	$\overline{EN}$ to IN	300			300			300				5
	SET MAX to LEN	800			800			800				
	SET MIN to LEN	800			800			800				
t_{jit}	Jitter		<5			<5			<5		ps	8
t_r	Rise/Fall Time										ps	
t_f	20 - 80% (Q)	125	225	325	125	225	325	125	225	325		
	20 - 80% (CASCADE)	300	450	650	300	450	650	300	450	650		

1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
2. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
3. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
4. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
5. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
6. Specifcation limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (ie. increasing delay steps for increasing binary counts on the control inputs Dn). Typically the device will be monotonic to the D0 input, however under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D0 input is the LSB. With the D1 input as the LSB the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

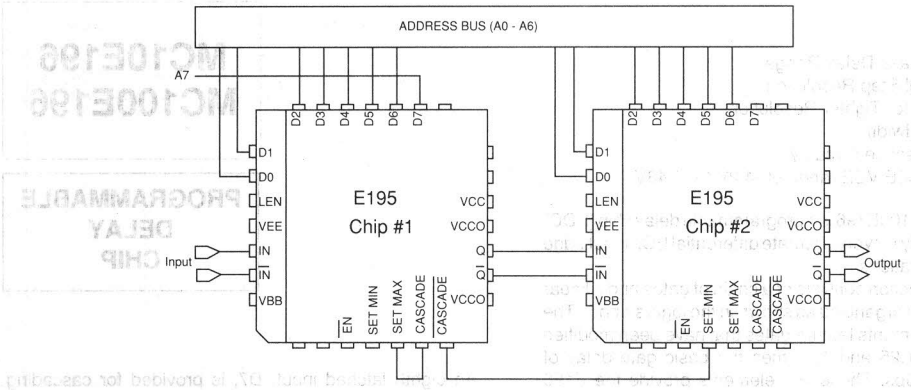


Figure 1 - Cascading Interconnect Architecture

Cascading Multiple E195's

To increase the programmable range of the E195 internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E195's without the need for any external gating. Furthermore this capability requires only one more address line per added E195. Obviously cascading multiple PDC's will result in a larger programmable range however this increase is at the expense of a longer minimum delay

Figure 1 illustrates the interconnect scheme for cascading two E195's. As can be seen, this scheme can easily be expanded for larger E195 chains. The D7 input of the E195 is the cacade control pin. With the interconnect scheme of Figure 1 when D7 is asserted it signals the need for a larger programmable range than is acheivable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding any changes on the A0-A6 address bus will not affect the operation of chip #2.

Chip #1 on the other hand will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0-A6. If the delay needed is greater than can be acheived with 31.75 gate delays (1111111 on the A0-A6 address bus) D7 will be asserted to signal the need to cascade the delay to the next E195 device. When D7 is asserted the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A0-A6 address bus. Chip #1 on the other hand will have its SET MAX pin asserted resulting in the device delay to be independent of the A0-A6 address bus.

When the SET MAX pin of chip #1 is asserted the D0 and D1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity an additional gate delay is selected in the cascade circuitry. As a result when D7 of chip #1 is asserted the delay increases from 31.75 gates to 32 gates. A 32 gate delay is the maximum delay setting for the E195.

To expand this cascading scheme to more devices one simply needs to connect the D7 input and CASCADE outputs of the current most significant E195 to the new most significant E195 in the same manner as pictured in figure 1. The only addition to the logic is the increase of one line to the address bus for cascade control of the second PDC.

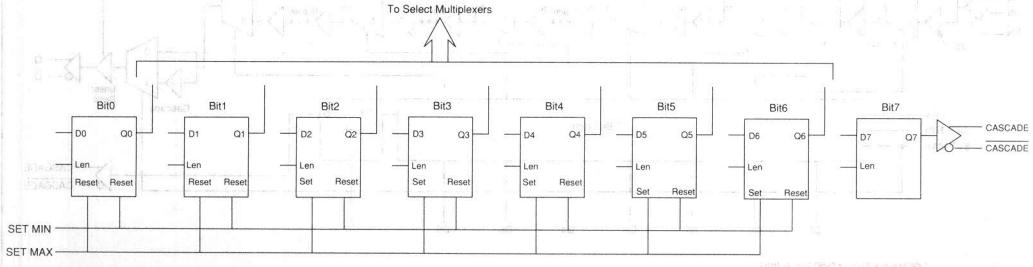


Figure 2 - Expansion of the Latch Section of the E195 Block Diagram

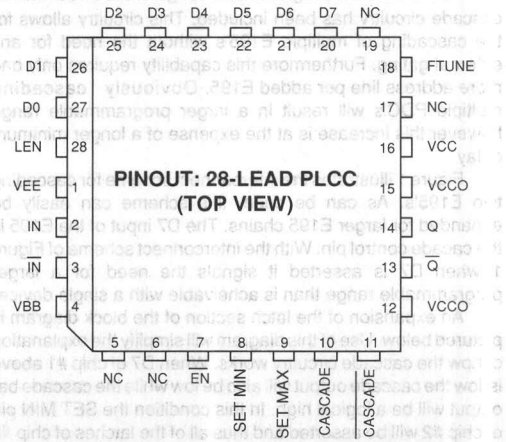
to have delays 1.25 and 1.5 times the basic gate delay of approximately 80ps. These two elements provide the E196 with a digitally-selectable resolution of approximately 20ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on chip by a high signal on the latch enable (LEN) control.

The FTUNE input takes an analog voltage and applies it to an internal linear ramp for reducing the 20ps resolution still further. The FTUNE input is what differentiates the E196 from the E195.

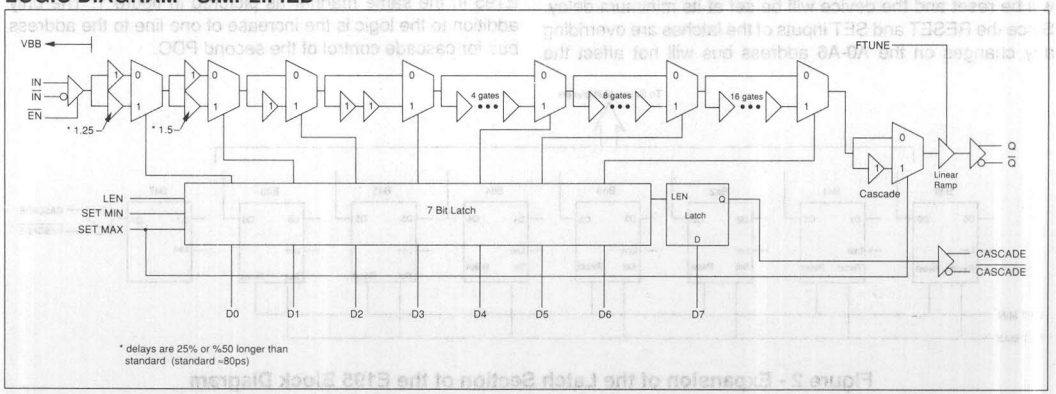
An eighth latched input, D7, is provided for cascading multiple PDC's for increased programmable range. The cascade logic allows full control of multiple PDC's, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

PIN NAMES

Pin	Function
$\overline{IN}$/IN	Signal Input
$\overline{EN}$	Input Enable
D[0:7]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Min Delay Set
SET MAX	Max Delay Set
CASCADE	Cascade Signal
FTUNE	Linear Voltage Input



LOGIC DIAGRAM - SIMPLIFIED



DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		130	156		130	156		130	156		
	100E		130	156		130	156		150	179		

3

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

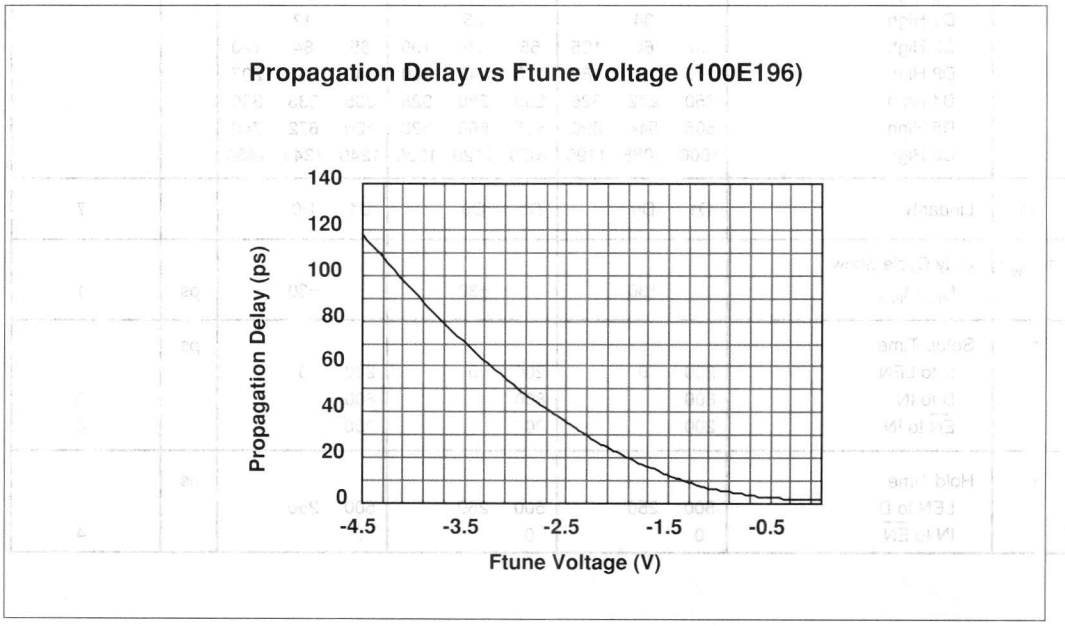
Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay										ps	
t_{PHL}	IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765		
	IN to Q; Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720		
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950		
	D7 to CASCADE	300	450	700	300	450	700	300	450	700		
t_{RANGE}	Programmable Range											
	t_{PD} (max) - t_{PD} (min)	2000	2175		2050	2240		2375	2580		ps	
Δt	Step Delay										ps	6
	D0 High		17			17.5			21			
	D1 High		34			35			42			
	D2 High	55	68	105	55	70	105	65	84	120		
	D3 High	115	136	180	115	140	180	140	168	205		
	D4 High	250	272	325	250	280	325	305	336	380		
	D5 High	505	544	620	515	560	620	620	672	740		
	D6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450		
Lin	Linearity	D1	D0		D1	D0		D1	D0			7
t_{SKEW}	Duty Cycle Skew											
	t_{PHL} - t_{PLH}		±30			±30			±30		ps	1
t_s	Setup Time										ps	
	D to LEN	200	0		200	0		200	0			
	D to IN	800			800			800				2
	$\overline{EN}$ to IN	200			200			200				3
t_h	Hold Time										ps	
	LEN to D	500	250		500	250		500	250			
	IN to $\overline{EN}$	0			0			0				4

AC Characteristics (Cont): $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

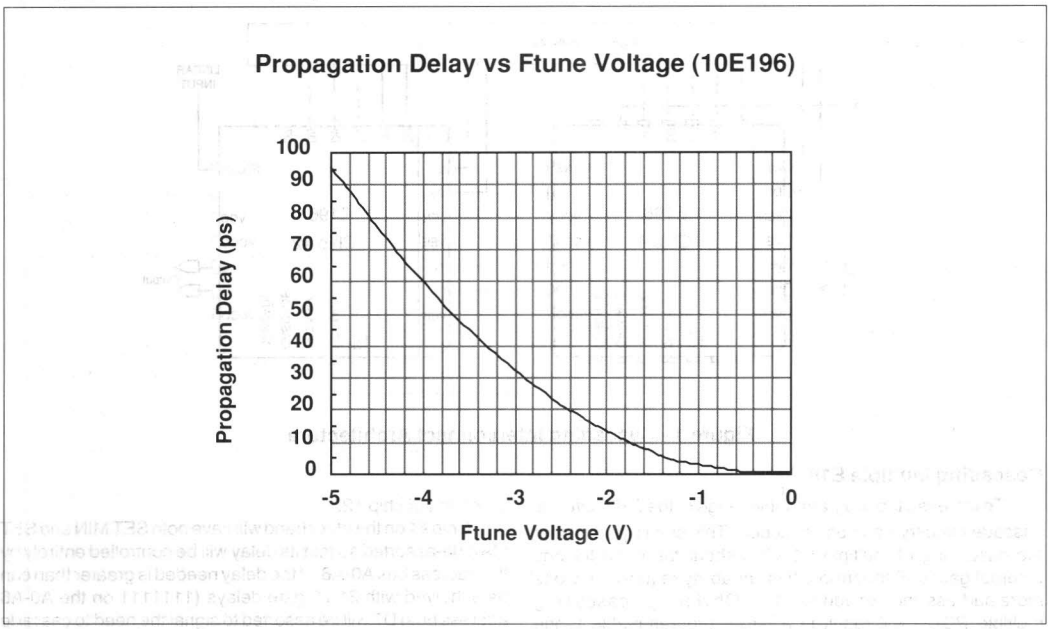
Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		min	typ	max	min	typ	max	min	typ	max		
t_R	Release Time										ps	
	$\overline{EN}$ to IN	300			300			300				5
	SET MAX to LEN	800			800			800				
	SET MIN to LEN	800			800			800				
t_{jit}	Jitter		<5			<5			<5		ps	8
t_r	Rise/Fall Time										ps	
t_f	20 - 80% (Q)	125	225	325	125	225	325	125	225	325		
	20 - 80% (CASCADE)	300	450	650	300	450	650	300	450	650		

1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
2. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
3. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
4. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
5. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
6. Specifcation limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (ie. increasing delay steps for increasing binary counts on the control inputs Dn). Typically the device will be monotonic to the D0 input, however under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D0 input is the LSB. With the D1 input as the LSB the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

Analog Input Characteristics: Ftune = VCC to VEE



Analog Input Characteristics (cont): Ftune = VCC to VEE



USING THE FTUNE ANALOG INPUT

The analog FTUNE pin on the E196 device is intended to enhance the 20ps resolution capabilities of the fully digital E195. The level of resolution obtained is dependent on the number of increments applied to the appropriate range on the FTUNE pin.

To provide another level of resolution the FTUNE pin must be capable of adjusting the delay by greater than the 20ps digital resolution. From the provided graphs one sees that this requirement is easily achieved as over the entire FTUNE voltage range a 100ps delay can be achieved. This extra analog range ensures that the FTUNE pin will be capable even under worst case conditions of covering the digital resolution.

Typically the analog input will be driven by an external DAC to provide a digital control with very fine analog output steps. The final resolution of the device will be dependent on the width of the DAC chosen.

To determine the voltage range necessary for the FTUNE input, the graphs provided should be used. As an example if a range of 40ps is selected to cover worst case conditions and ensure coverage of the digital range, from the 100E196 graph a voltage range of -3.25V to -4V would be necessary on the FTUNE pin. Obviously there are numerous voltage ranges which can be used to cover a given delay range, users are given the flexibility to determine which one best fits their designs.

Applications Information

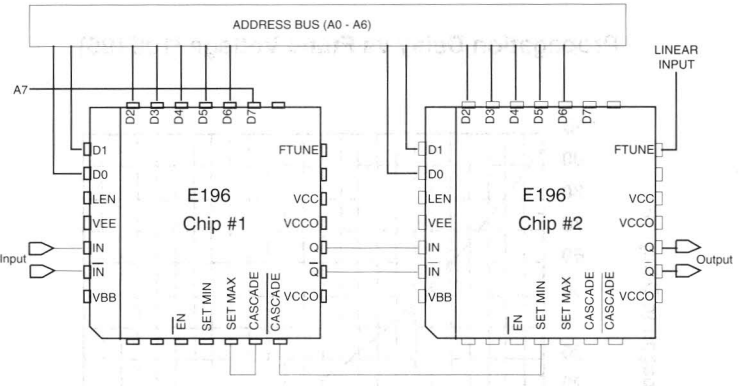


Figure 1 - Cascading Interconnect Architecture

Cascading Multiple E196's

To increase the programmable range of the E196 internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E196's without the need for any external gating. Furthermore this capability requires only one more address line per added E196. Obviously cascading multiple PDC's will result in a larger programmable range however this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E196's. As can be seen, this scheme can easily be expanded for larger E196 chains. The D7 input of the E196 is the cacade control pin. With the interconnect scheme of Figure 1 when D7 is asserted it signals the need for a larger programmable range than is acheivable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding any changes on the A0-A6 address bus will not affect the operation of chip #2.

Chip #1 on the other hand will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0-A6. If the delay needed is greater than can be acheived with 31.75 gate delays (1111111 on the A0-A6 address bus) D7 will be asserted to signal the need to cascade the delay to the next E196 device. When D7 is asserted the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A0-A6 address bus. Chip #1 on the other hand will have its SET MAX pin asserted resulting in the device delay to be independent of the A0-A6 address bus.

When the SET MAX pin of chip #1 is asserted the D0 and D1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity an additional gate delay is selected in the cascade circuitry. As a result when D7 of chip #1 is asserted the delay increases from 31.75 gates to 32 gates. A 32 gate delay is the maximum delay setting for the E196.

When cacsading multiple PDC's it will prove more cost effective to use a single E196 for the MSB of the chain while using E195 for the lower order bits. This is due to the fact that only one fine tune input is needed to further reduce the delay step resolution.

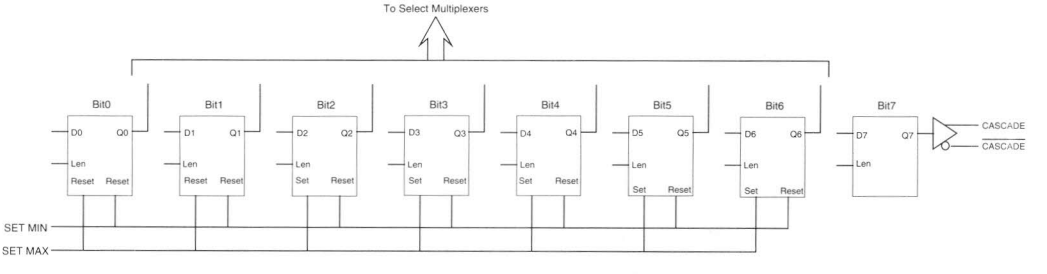


Figure 2 - Expansion of the Latch Section of the E195 Block Diagram

MC10E197

Data Separator

3

Advanced Information

- 2:7 and 1:7 RLL Format Compatible
- Fully Integrated VCO for 50Mb/s Operation
- External VCO Input for Higher Operating Frequency
- Anti-equivocation Circuitry to Ensure PLL Lock

The MC10E197 is an integrated data separator designed for use in high speed hard disk drive applications. With data rate capabilities of up to 50Mb/s the device is ideally suited for today's and future state-of-the-art hard disk designs.

The E197 is typically driven by a pulse detector which reads the magnetic information from the storage disk and changes it into ECL pulses. The device is capable of operating on both 2:7 and 1:7 RLL coding schemes. Note that the E197 does not do any decoding but rather prepares the disk data for decoding by another device.

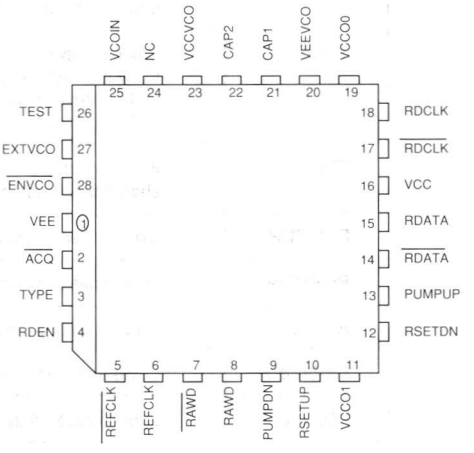
For applications with higher data rate needs, such as tape drive systems, the device accepts an external VCO. The frequency capability of the integrated VCO is the factor which limits the device to 50Mb/s.

A special anti-equivocation circuit has been employed to ensure timely lock-up when the arriving data and VCO edges are coincident.

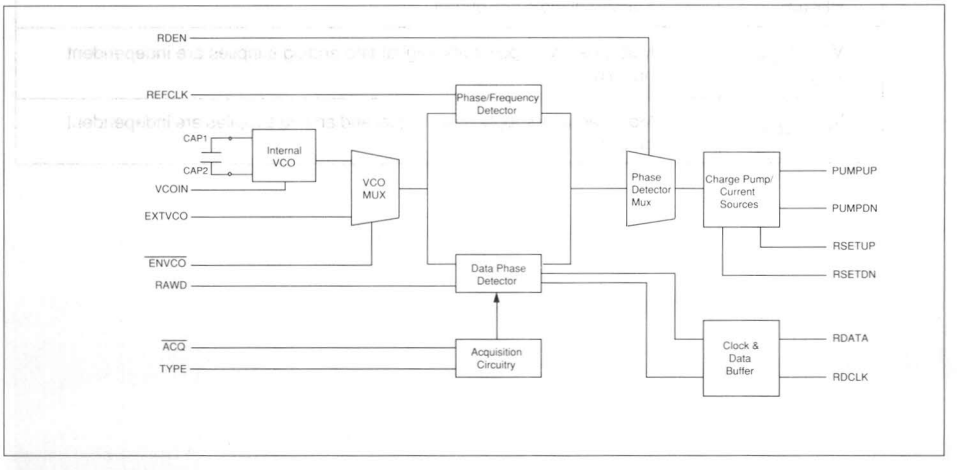
Unlike the majority of the devices in the ECLinPS family, the E197 is available in only 10KH compatible ECL. The device is available in the standard 28-lead PLCC.

Since the E197 contains both analog and digital circuitry, separate supply and ground pins have been provided to minimize noise coupling inside the device. The device can operate on either standard negative ECL supplies or as is more common on positive voltage supplies.

PINOUT: 28-Lead PLCC (TOP VIEW)



LOGIC SYMBOL



This document contains information on a new product. Specifications and information herein are subject to change without notice.

Pin Description

REFCLK	Reference clock equivalent to one clock cycle per decoding window.
RDEN	Enable data synchronizer when HIGH. When LOW enable the phase/ frequency detector steered by REFCLK.
RAWD	Data Input to Synchronizer logic.
VCOIN	VCO control voltage input
CAP1/CAP2	VCO frequency controlling capacitor inputs
$\overline{\text{ENVCO}}$	VCO select pin. LOW selects the internal VCO and HIGH selects the external VCO input. Pin floats LOW when left open.
EXTVCO	External VCO pin selected when ENVCO is HIGH
$\overline{\text{ACQ}}$	Aquisistion circuitry select pin. This pin must be driven HIGH at the end of the data sync field for some sync field types.
TYPE	Selects between the two types of commonly used sync fields. When LOW it selects a sync field interspersed with 3 zeroes (2:7 RLL code). When HIGH it selects a sync field interspersed with 2 zeroes (1:7 RLL code).
TEST	Input included to initialize the clock flip-flop for test purposes only. Pin should be left open (LOW) in actual application.
PUMPUP	Open collector charge pump output for the signal pump
PUMPDN	Open collector charge pump output for the reference pump
RSETUP	Current setting resistor for the signal pump
RSETDN	Current setting resistor for the reference pump
RDATA	Synchronized data output
RDCLK	Synchronized clock output
V_{CC}, V_{CCO}, V_{CCVCO}	Most positive supply rails. Digital and analog supplies are independent on chip
V_{EE}, V_{EEVCO}	Most negative supply rails. Digital and analog supplies are independent on chip

I_{OUT}	Charge Pump Output Leakage Current		1		1		1	µA	3	
V_{ACT}	PUMPUP/PUMPDN Active Voltage Range	V_{CC}-2.5	V_{CC}	V_{CC}-2.5	V_{CC}	V_{CC}-2.5	V_{CC}	V		

10 KH LOGIC LEVELS

DC Characteristics: $V_{EE} = V_{EE}$(min) to V_{EE}(max); $V_{CC} = V_{CCO} = V_{CCO1} = V_{CCVCO}$ = GND

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
V_{OH}	Output HIGH Voltage	-1020		-840	-980		-810	-910		-720	mV	
V_{OL}	Output LOW Voltage	-1950		-1630	-1950		-1630	-1950		-1595	mV	
V_{IH}	Input HIGH Voltage	-1170		-840	-1130		-810	-1060		-720	mV	
V_{IL}	Input LOW Voltage	-1950		-1480	-1950		-1480	-1950		-1445	mV	

POSITIVE EMITTER COUPLED LOGIC LEVELS

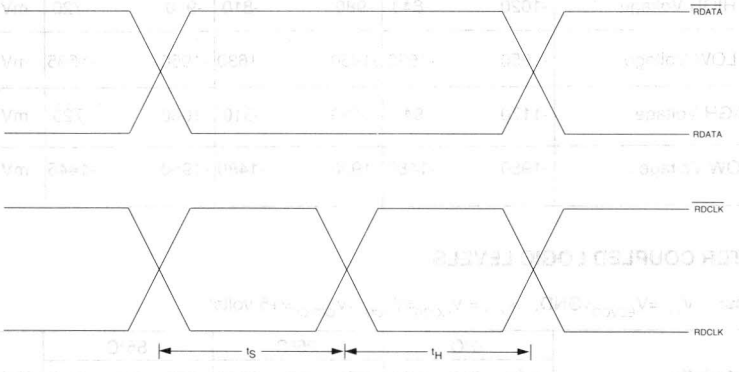
DC Characteristics: $V_{EE} = V_{EEVCO}$=GND; $V_{CC} = V_{CCO0} = V_{CCO1} = V_{CCVCO}$=+5 volts*

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
V_{OH}	Output HIGH Voltage	3980		4160	4020		4190	4090		4280	mV	
V_{OL}	Output LOW Voltage	3050		3370	3050		3370	3050		3405	mV	
V_{IH}	Input HIGH Voltage	3830		4160	3870		4190	3940		4280	mV	
V_{IL}	Input LOW Voltage	3050		3520	3050		3050	3050		3555	mV	

*V_{OH} and V_{OL} levels will vary 1:1 with V_{CC}

f_{VCO}	Frequency of the VCO							
	Tuning Ratio	1.53	1.87	1.53	1.87	1.53	1.87	6

1. Applies to the input current for each input except VCOIN
2. For a nominal set current of 3.72 mA, the resistor values for RSETUP and RSETDN should be 130Ω(0.1%). Assuming no variation between these two resistors the current match between the PUMPUP and PUMPDN output signals should be within ±3%. I_{SET} is calculated as $(V_{EE} + 1.3v - V_{BE})/R$; where R is RSETUP or RSETDN and a nominal value for V_{BE} is 0.85 volts.
3. Output leakage current of the PUMPUP or PUMPDN output signals when at a LOW level.
4. T_{VCO} is the period of the VCO.
5. The VCO frequency determined with VCOIN = V_{EE} + 0.5volts and using a 10pF tuning capacitor.
6. The tuning ratio is defined as the ratio of f_{VCOMAX} to f_{VCOMIN}, where f_{VCOMAX} is measured at VCOIN = 1.3v + V_{EE} and f_{VCOMAX} is measured at VCOIN = 2.6v + V_{EE}.
7. Setup and hold timing diagrams:



Applications Information

General Operation

Operation

The E197 is a phase-locked loop circuit consisting of an internal VCO, a Data Phase detector with associated acquisition circuitry, and a Phase/Frequency detector(Fig. 1). In addition, an enable pin(ENVCO) is provided to disable the internal VCO and enable the external VCO input. Hence, the user has the option of supplying the VCO signal.

The E197 contains two phase detectors: a data phase detector for synchronizing to the non-periodic pulses in the read data stream during the data read mode of operation, and a phase/frequency detector for frequency (and phase) locking to an external reference clock during the "idle" mode of operation. The read enable (RDEN) pin muxes between these two detectors.

Data Read Mode

The data pins (RAWD) are enabled when the RDEN pin is placed at a logic high level, thus enabling the Data Phase detector(Fig. 1) and initiating the data read mode. In this mode the loop is servoed by the timing information taken from the positive edges of the input data pulses. This phase detector samples positive edges from the RAWD signal and generates both a pump up and pump down pulse from any edge of the input data pulse. The leading edge of the pump up pulse is time modulated by the leading edge of the data signal, whereas the rising edge of the pump up pulse is generated synchronous to the VCO clock. The falling edge of the pump down pulse is synchronous to the rising edge of the VCO clock and the rising edge of the pump down signal is synchronous to the falling edge of the VCO clock. Since both edges of the VCO are used the internal clock a duty cycle of 50%. This pulse width modulation technique is used to generate the servoing signal which drives the VCO. The pump down signal is a reference pulse which is included to provide an evenly balanced differential system, thereby allowing the synthesis of a VCO input control signal after appropriate signal processing by the loop filter.

By using suitable external filter circuitry, a control signal for input into the VCO can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when the data edges lead the clock by a half clock cycle. If the data edges are advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a negative polarity; whereas if the VCO is advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a positive polarity. If there is no data edge present at the RAWD input, the corresponding pump up and pump down outputs are not generated and the resulting control output is zero.

Acquisition Circuitry

The acquisition circuitry is provided to assist the data phase detector in phase locking to the sync field that precedes the data. For the case in which lock-up is attempted when the data edges are coincident with the VCO edges, the pump down signal may enter an indeterminate state for an unacceptably long period due to the violation of internal set up and hold times. After an initial pump down pulse, the circuit blocks successive pump down pulses, and inserts extra pump up pulses, during portions of the sync field that are known to contain zeros. Thus the data phase detector is forced to have a nonzero output during the lock-up period, and the restoring force ensures correction of the loop within an acceptable time. Hence, this circuitry provides a quasi-deterministic pump down output signal, under the condition of coincident data and VCO edges, allowing lock-up to occur without excessive delays.

The ACQ line is provided to disable(disable = HIGH) the acquisition circuit during the data portion of a sector block. Typically, this circuit is enabled at the beginning of the sync field by a one-shot timer to ensure a timely lock-up.

The TYPE line allows the choice between two sync field preamble types: transitions interspersed with two zeros between transitions, or three zeros between transitions. These types of sync fields are used with the 1:7 and 2:7 RLL coding schemes, respectively.

3

Idle Mode

In the absence of data or when the drive is writing to the disk, PLL servoing is accomplished by pulling the read enable line (RDEN) low and providing a reference clock via the REFCLK pins. The condition whereby RDEN is low selects the Phase/Frequency detector(Fig. 1) and the 10E197 is said to be operating in the "idle mode." In order to function as a frequency detector the input waveform must be periodic. The pump up and pump down pulses from the Phase/Frequency detector will have the same frequency, phase and pulse width only when the two clocks that are being compared have their positive edges aligned and are of the same frequency.

As with the data phase detector, by using suitable external filter circuitry, a VCO input control signal can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when all positive edges of both clocks are coincident. For the case in which the frequencies of the two clocks are the same but the clock edges of the reference clock are slightly advanced with respect to the VCO clock, the control signal is defined to have a positive polarity. A control signal with negative polarity occurs when the edges of the reference clock are delayed with respect to those of the VCO. If the frequencies of the two clocks are different, the clock with the most edges per unit time will initiate the most pulses and the polarity of the detector will reflect the frequency error. Thus, when the reference clock is higher in frequency than the VCO clock the polarity of the control signal is positive; whereas a control signal with negative polarity occurs when the frequency of the reference clock is lower than the VCO clock.

Phase Lock Loop Theory

Introduction

Phase lock loop (PLL) circuits are fundamentally feedback systems used to synchronize the frequency of an oscillator to an incoming signal. In addition to frequency synchronization, the PLL circuitry is designed to minimize the phase difference between the system input and output signals. A block diagram of a feedback control system is shown in Figure 1.

where:

A(s) is the product of the feed-forward transfer functions.

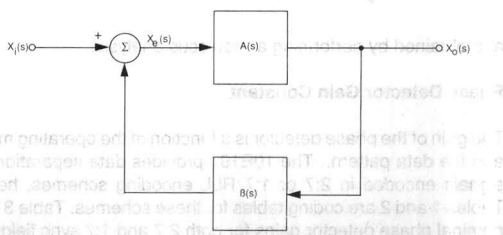


Figure 1 - Feedback System

ß(s) is the product of the feedback transfer functions.

The transfer function for this closed loop system is

$$\frac{X_o(s)}{X_i(s)} = \frac{A(s)}{1 + A(s)ß(s)}$$

Typically, phase lock loops are modeled as feedback systems connected in a unity feedback configuration(ß(s)=1) with a phase detector, a VCO(voltage controlled oscillator), and a loop filter in the feed-forward path, A(s). Figure 2 illustrates a phase lock loop as a feedback control system in block diagram form.

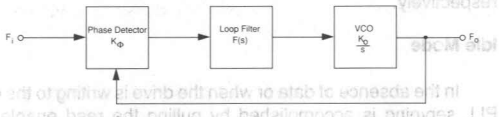


Figure 2 - Phase Lock Loop Block Diagram

The closed loop transfer function is:

$$\frac{X_o(s)}{X_i(s)} = \frac{K_\phi \frac{K_o}{s} F(s)}{1 + K_\phi \frac{K_o}{s} F(s)}$$

where:

K_ϕ= the phase detector gain.

K_o= the VCO gain. Since the VCO introduces a pole at the origin of the s-plane, K_o is divided by s.

F(s) = the transfer function of the loop filter.

The 10E197 is designed to implement the phase detector and VCO functions in a unity feedback loop, while allowing the user to select the desired filter function.

Gain Constants

As mentioned, each of the three sections in the phase lock loop block diagram has an associated open loop gain constant. Further, the gain constant of the filter circuitry is composed of the product of three gain constants, one for each filter subsection. The open loop gain constant of the feed-forward path is given by

$$K_{ol} = K_\phi * K_o * K_1 * K_l * K_d \qquad \text{eqt. 1}$$

and obtained by performing a root locus analysis.

Phase Detector Gain Constant

The gain of the phase detector is a function of the operating mode and the data pattern. The 10E197 provides data separation for signals encoded in 2:7 or 1:7 RLL encoding schemes; hence Tables 1 and 2 are coding tables for these schemes. Table 3 lists nominal phase detector gains for both 2:7 and 1:7 sync fields.

NRZ Data Sequence	Code Sequence
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Table 1 - 2:7 RLL Encoding Table

NRZ Data Sequence	Code Sequence
00	X01
01	010
10	X00
1100	010001
1101	X00000
1110	X00001
1111	010000

An X in the leading bit of a code sequence is assigned the complement of the bit

Table 2 - 1:7 RLL Encoding Table

Sync Pattern	Read Mode	Idle Mode
2:7	121 mV/radian	484 mV/radian
1:7	161 mV/radian	483 mV/radian

Table 3 - Phase Detector Gain Constants

VCO Gain Constant

The gain of the VCO is a function of the tuning capacitor. For a value of 10 pF a nominal value of the gain,K_o,is 20MHz per volt.

Filter Circuitry Gain Constant(s)

The open loop gain constant of the filter circuitry is given by:

$$K_{fc} = K_1 * K_l * K_d \qquad \text{eqt. 2}$$

The individual gain constants are defined in the appropriate subsections of this document.

Loop Filter

The two major functions of the loop filter are to remove any noise or high frequency components present in the phase detector output signal, and more importantly to control the characteristics which determine the dynamic response of the phase lock loop i.e. capture range, loop bandwidth, capture time, and transient response.

Although a variety of loop filter configurations exist, this section will only describe a filter capable of performing the signal processing as described in the Data Read Mode and the Idle Mode sections. The loop filter consists of a differential summing amplifier cascaded with an augmenting integrator which drives the VCOIN input to the 10E197 through a resistor divider network(Fig. 3).

The transfer function and the element values for the loop filter are derived by dividing the filter into three cascaded subsections: filter input, augmenting integrator, and the voltage divider network(Fig.4).

Loop Filter Transfer Function

The open loop transfer function of the phase lock loop is the product of each individual filter subsection, as well as the phase detector and VCO. Thus, the open loop filter transfer function is:

$$F_o(s) = K_\phi * \frac{K_o}{s} * F_1(s) * F_I(s) * F_d(s)$$

where:

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{01})s + \omega_{01}^2]}$$

$$F_I(s) = K_I * \frac{1}{s} * \frac{(s + z)}{[s^2 + (2\zeta\omega_{02})s + \omega_{02}^2]}$$

$$F_d(s) = K_d * \frac{1}{(s + p_2)}$$

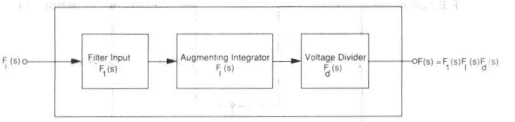


Figure 4 - Loop Filter Block Diagram

A root locus analysis is performed on the open loop transfer function to determine the final pole-zero locations and the open loop gain constant for the phase lock loop. Note that the open loop gain constant impacts the crossover frequency and that a lower frequency crossover point means a much more efficient filter. Once these positions and constants are determined the component values may be calculated.

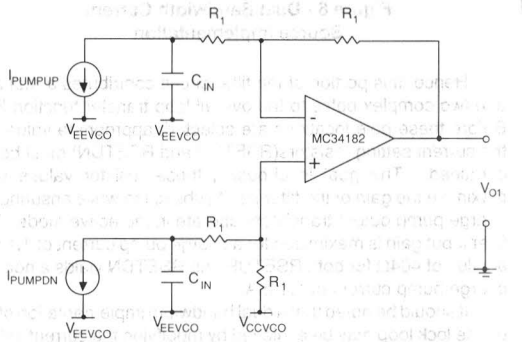


Figure 5 - Filter Input Sunsection

Filter Input

The primary function of the filter input subsection is to convert the output of the phase detector into a single ended signal for subsequent processing by the integrator circuitry. This subsection consists of the 10E197 charge pump current sinks, two shunt capacitors, and a differential summing amplifier(Fig. 5).

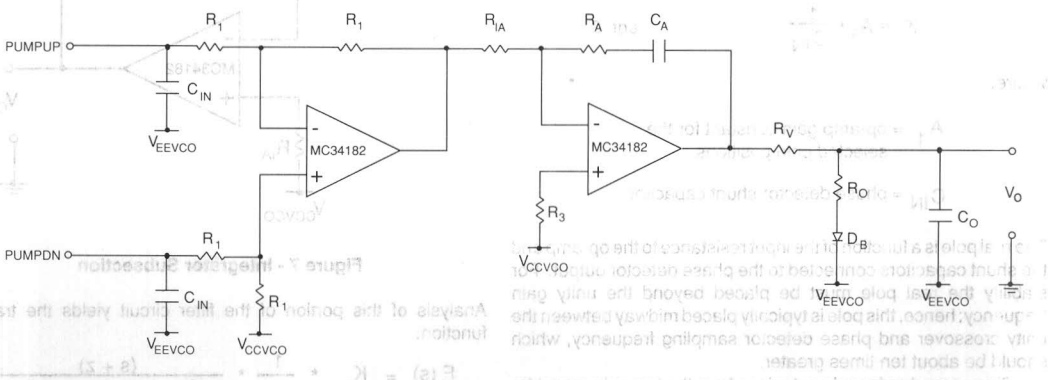


Figure 3 - Loop Filter Circuitry

Figure 6 - Dual Bandwidth Current Source Implementation

Hence, this portion of the filter circuit contributes a real pole and two complex poles to the overall loop transfer function F(s). Before these pole locations are selected, appropriate values for the current setting resistors(RSETUP and RSETDN) must be ascertained. The goal in choosing these resistor values is to maximize the gain of the filter input subsection while ensuring the charge pump output transistors operate in the active mode. The filter input gain is maximized for a charge pump current of 1.1 mA; a value of 464Ω for both RSETUP and RSETDN yields a nominal charge pump current of 1.1 mA.

It should be noted that a dual bandwidth implementation of the phase lock loop may be achieved by modifying the current setting resistors such that an electronic switch enables one of two resistor configurations. Figure6 shows a circuit configuration capable of providing this dual bandwidth function. Analysis of the filter input circuitry yields the transfer function:

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{01})s + \omega_{01}^2]}$$

The gain constant is defined as:

$$K_1 = A_1 * \frac{1}{C_{IN}} \qquad \text{eqt. 3}$$

where:

A_1 = op-amp gain constant for the selected pole positions.

C_{IN} = phase detector shunt capacitor.

The real pole is a function of the input resistance to the op-amp and the shunt capacitors connected to the phase detector output. For stability the real pole must be placed beyond the unity gain frequency; hence, this pole is typically placed midway between the unity crossover and phase detector sampling frequency, which should be about ten times greater.

The second order pole set arises from the two pole model for an op-amp. The open loop gain and the first open loop pole for the unity gain operation. Performing a root locus analysis on the op-amp open loop configuration and adhering to the two constraints yields the pole positions contributed by the op-amp.

Determination of Element Values

Since the difference amplifier is configured to operate as a differential summer the resistor values associated with the amplifier are of equal value. Further, the typical input resistance to the summing amplifier is 1 kΩ; thus the op-amp resistors are set at 1 kΩ. Having set the input resistance to the op-amp and selected the position of the real pole, the value of the shunt capacitors is determined using the following relationship:

$$|p_1| = \frac{1}{2\pi R_1 C_{IN}} \qquad \text{eqt. 4}$$

Augmenting Integrator

The augmenting integrator consists of an active filter with a lag-lead network in the feedback path(Fig. 7).

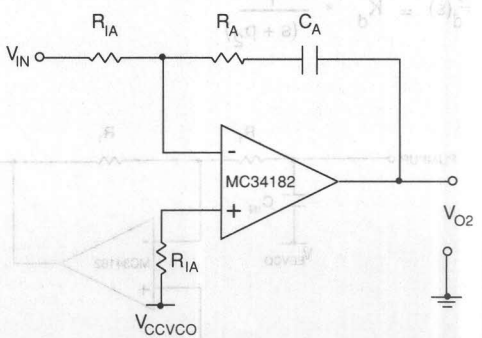


Figure 7 - Integrator Subsection

Analysis of this portion of the filter circuit yields the transfer function:

$$F_1(s) = K_1 * \frac{1}{s} * \frac{(s + z)}{[s^2 + (2\zeta\omega_{02})s + \omega_{02}^2]}$$

The gain constant is defined as:

$$K_I = A_I * \frac{R_A}{R_{IA}} \qquad \text{eqt. 5}$$

where:

A_I = op-amp gain constant for selected pole positions.

R_A = integrator feedback resistor.

R_{IA} = integrator input resistor.

The integrator circuit introduces a zero, a pole at the origin, and a second order pole set as described by the two pole model for an op-amp. As in the case of the differential summing amplifier, we assume the op-amp pole pair occur as a complex conjugate pair making an angle of 45° to the real axis of the complex frequency plane; are positioned for near unity gain operation; and are located beyond the crossover frequency. Since both the summing and integrating op-amps are realized by the same type of op-amp(MC34182D), the open loop pole positions for both amplifiers will be the same.

Further, the loop transfer function contains two poles located at the origin, one introduced by the integrator and the other by the VCO; hence a zero is necessary to compensate for the phase shift produced by these poles and ensure loop stability. The op-amp will be stable if the crossover point occurs before the transfer function phase angle becomes 180°. The zero should be positioned much less than one decade before the unity gain frequency.

As in the case of the filter input circuitry, the poles and zero from this analysis will be used as open loop poles and a zero when performing the root locus analysis for the complete system.

Determination of Element Values

The location of the zero is used to determine the element values for the augmenting integrator. The value of the capacitor, C_A, is selected to provide adequate charge storage when the loop is not sampling data. A value of 0.1μF is sufficient for most applications; this value may be increased when the RDCLK frequency is much lower than 4 MHz. The value of R_A is governed by:

$$|z| = \frac{1}{2\pi R_A C_A} \qquad \text{eqt. 6}$$

For unity gain operation of the integrating op-amp the value of R_{IA} is selected such that:

$$R_{IA} = R_A \qquad \text{eqt. 7}$$

It should be noted that although the zero can be tuned by varying either R_A or C_A, caution must be exercised when adjusting the zero by varying C_A because the integrator gain is also a function of C_A. Further, the gain of the loop filter can be adjusted by changing the integrator input resistor R_{IA}.

Voltage Divider

The input range to the VCOIN input is from 1.3v + V_{EE} to 2.6v + V_{EE}, hence the output from the augmenting amplifier section must be attenuated to meet the VCOIN constraints. A simple voltage divider network provides the necessary attenuation(Fig. 8).

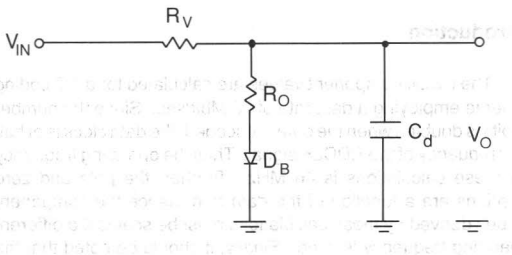


Figure 8 - Voltage Divider Subsection

In addition, a shunt filter capacitor connected between the VCOIN input pin and V_{EE} provides the voltage divider subsection with a single time constant transfer function that adds a pole to the overall loop filter. The transfer function for the voltage divider network is:

$$F_d(s) = K_d * \frac{1}{(s + p_2)}$$

The gain constant, K_d, is defined as:

$$K_d = \frac{1}{R_v C_d} \qquad \text{eqt. 9}$$

The value of K_d is easily extracted by rearranging Equation 1:

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_I} \qquad \text{eqt. 10}$$

The gain constant K_d is set such that the output from the integrator circuit is within the range 1.3v +VEE to 2.6v +VEE.
The pole for the voltage divider network should be positioned an octave beyond that for the filter input.

Determination of Element Values

Once the pole location and the gain constant K_d are established the resistor values for the voltage divider network are determined using the design guidelines mentioned above and from the following relationship:

$$\frac{K_d}{2\pi |p_2|} = \frac{R_o}{R_o + R_V}$$

Having determined the resistor values, the filter capacitor is calculated by rearranging Equation 9:

$$C_d = \frac{1}{R_v K_d} \qquad \text{eqt. 9a}$$

Finally, a bias diode is included in the voltage divider network to provide temperature compensation. The finite resistance of this diode is neglected for these calculations.

Calculations For a 2:7 Coding Scheme

Introduction

3

The circuit component values are calculated for a 2:7 coding scheme employing a data rate of 23 Mbit/sec. Since the number of bits is doubled when the data is encoded, the data clock is at half the frequency of the RDCLK signal. Thus the operating frequency for these calculations is 46 MHz. Further, the pole and zero positions are a function of the data rate, hence the component values derived by these calculations must be scaled if a different operating frequency is used. Finally, it should be noted that the values are optimized for settling time.

The analysis is divided into three parts: static pole positioning, dynamic pole positioning, and dynamic zero positioning. Dynamic poles and zeros are those which the designer may position, to yield the desired dynamic response, through the judicious choice of element values. Static poles are not directly controlled by the choice of component values.

Static Poles

Each op-amp introduces a pair of "static" complex conjugate poles which must lie beyond the crossover frequency. As obtained from the data sheets and laboratory measurements the two open loop poles for the MC34182D are:

$$P^*_{1a} = -0.1 \text{ Hz}$$

$$P^*_{1b} = -11.2 \text{ Hz}$$

Performing a root locus analysis and following the two guidelines previously stated, an acceptable pole set is:

$$P_{1a} = -5.65 + j5.65 \text{ MHz}$$

$$P_{1b} = -5.65 - j5.65 \text{ MHz}$$

Both op-amps introduce a set of static complex conjugate poles at these positions for a total of four poles. Further, the loop gain for each op-amp associated with these pole positions is determined from the root locus analysis to be:

$$A_1 = A_2 = 2.48 \text{ e}15 \ \frac{V}{V}$$

In addition to the op-amps, the integrator and the VCO each contribute a static pole at the origin. Thus, there are a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned midway between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

$$P^*_1 = -1.24 \text{ MHz}$$

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus the open loop voltage divider pole position is picked to be:

$$P^*_2 = -2.57 \text{ MHz}$$

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency; for this design the zero is placed at:

$$z = -311 \text{ Hz}$$

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot; if the phase margin is not sufficient, the dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions the component values are calculated. From the root locus analysis the dynamic pole and zero positions are:

$$P_1 = -573 \text{ kHz}$$

$$P_2 = -3.06 \text{ MHz}$$

$$z = -311 \text{ Hz}$$

Filter Input Subsection

Rearranging Equation 4:

$$C_{IN} = \frac{1}{2\pi R_1 |p_1|}$$

and substituting 573 kHz for the pole position and 1 kΩ for the resistor value yields:

$$R_{IA} = R_A = 5.11\ k\Omega$$

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9, and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3v + V_{EE} to 2.6v + V_{EE}.
Restating Equation 9,

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_I}$$

From the root locus analysis K_{ol} is determined to be:

$$K_{ol} = 1.585\ e51\ \frac{V}{mA\ sec^3}$$

From Equation 3

$$K_1 = A_1 * \frac{1}{C_{IN}}$$

and the gain constant K_1 is:

$$K_1 = 8.90\ e21\ \frac{V}{mA\ sec}$$

From Equation 5

$$K_I = A_I * \frac{R_A}{R_{IA}}$$

and the gain constant K_I is:

$$K_I = 2.48\ e15\ \frac{V}{V}$$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_v\ K_d} \qquad \text{eqt. 8a}$$

the capacitor value, C_d is:

$$C_d = 98\ pF$$

Note that the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 23 Mbit/sec. If the data rate is different from the nominal design value the reactive elements must be scaled accordingly. The following equations are provided to facilitate scaling and were derived with the assumptions that a 2:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock.

$$C_{IN} = 278 * \frac{46}{f} \quad (pF) \qquad \text{eqt. 11}$$

$$C_d = 98 * \frac{46}{f} \quad (pF) \qquad \text{eqt. 12}$$

where f is the RDCLK frequency in MHz.

Example for an 11Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 2:7 code are used but the data rate is 11 Mbit/sec. The dynamic pole positions, and therefore the bandwidth of the loop filter, are a function of the data rate. Thus a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 11 the value of C_{IN} is:

Integrator Subsection:

$C_A = 0.1\ \mu F$

$R_A = 5.11\ k\Omega$

$R_{IA} = 5.11\ k\Omega$

$P_2 = -1.47\ MHz$

And, the open loop filter unity crossover point is at 300 kHz. The gain can be adjusted by changing the value of R_{IA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affect the dynamic performance of the filter.

Calculations For a 1:7 Coding Scheme

Introduction

The circuit component values are calculated for a 1:7 coding scheme employing a data rate of 20 Mbit/sec. Since the number of bits increases from two to three when the data is encoded, the data clock is at two-thirds the frequency of the RDCLK signal. Thus the operating frequency for these calculations is 30 MHz. As in the case of the 2:7 coding scheme the pole and zero positions are a function of the data rate, hence the component values derived by these calculations must be scaled if a different operating frequency is used.

Again, the analysis is divided into three parts: static pole positioning, dynamic pole positioning, and dynamic zero positioning.

Static Poles

As in the 2:7 coding example, an MC34182D op-amp is employed, hence the pole set is:

$$P_{1a} = -5.65 + j5.65\ MHz$$

$$P_{1b} = -5.65 - j5.65\ MHz$$

and the open loop gain is:

$$A_1 = A_2 = 2.48\ e15\ \frac{V}{V}$$

Since the op-amps introduce a set of complex conjugate poles, a total of four poles are introduced by the op-amp. In addition, the integrator and the VCO each contribute a pole at the origin for a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned midway between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

$$P_1^* = -1.1\ MHz$$

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus the open loop voltage divider pole position is selected as:

$$P_2^* = -2.28\ MHz$$

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency; for this design the zero is placed at:

$$z = -311\ Hz$$

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot; if the phase margin is not sufficient, the dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions the component values are calculated. From the root locus analysis the dynamic pole and zero positions are:

$$P_1 = -541 \text{ kHz}$$
$$P_2 = -2.73 \text{ MHz}$$
$$z = -311 \text{ Hz}$$

Filter Input Subsection

Rearranging Equation 4

$$C_{IN} = \frac{1}{2\pi R_1 |p_1|}$$

and substituting 541 kHz for the pole position and 1 kΩ for the resistor value yields:

$$C_{IN} = 294 \text{ pF}$$

Augmenting Integrator Subsection

Rearranging Equation 6:

$$R_A = \frac{1}{2\pi |z| C_A}$$

and substituting 311 Hz for the zero position and 0.1 μF for the capacitor value yields:

$$R_A = 5.11 \text{ k}\Omega$$

From Equation 7 the value for the other resistors associated with the integrator op-amp are set equal to R_A:

$$R_{IA} = R_A = 5.11 \text{ k}\Omega$$

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9, and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3v + V_{EE} to 2.6v + V_{EE}.
Restating Equation 9,

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_I}$$

From the root locus analysis K_{ol} is determined to be:

$$K_{ol} = 1.258 \text{ e}51 \ \frac{V}{mA \text{ sec}^3}$$

From Equation 3:

$$K_1 = A_1 * \frac{1}{C_{IN}}$$

and the gain constant K_1

$$K_1 = 8.42 \text{ e}21 \ \frac{V}{mA \text{ sec}}$$

From Equation 5:

$$K_I = A_I * \frac{R_A}{R_{IA}}$$

and the gain constant K_I is:

$$K_I = 2.48 \text{ e}15 \ \frac{V}{V}$$

$$K_d = 2.98 \text{ e}6 \ \text{sec}^{-1}$$

Having determined the gain constant K_d, the value of R_v is selected such that the constraints $R_v > R_o$ and:

$$\frac{K_d}{2\pi |p_2|} = \frac{R_o}{R_o + R_V}$$

are fulfilled. The pole position P_2 is determined from the root locus analysis to be:

$$P_2 = -2.73 \text{ MHz}$$

Hence, R_v is selected to be:

$$R_v = 2.15 \text{ k}\Omega$$

and R_o is calculated to be:

$$R_o = 453 \ \Omega$$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_v K_d} \qquad \text{eqt. 8a}$$

the capacitor value C_d is calculated to be:

$$C_d = 156 \text{ pF}$$

Again, note the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 20 Mbit/sec. If the data rate is different from the nominal design value the reactive elements must be scaled accordingly. The following equations are provided are to facilitate scaling and were derived with the assumptions that a 1:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock:

$$C_{IN} = 294 * \frac{30}{f} \quad (pF) \qquad \text{eqt. 13}$$

$$C_d = 156 * \frac{30}{f} \quad (pF) \qquad \text{eqt. 14}$$

where f is the RDCLK frequency in MHz.

Example for an 10 Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 1:7 code are used but the data rate is 10 Mbit/sec. The dynamic pole positions, and therefore the bandwidth of the loop filter,are a function of the data rate. Thus a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 13 the value of C_{IN} is:

$$C_{IN} = 588 \text{ pF}$$

and from Equation 14 the value of C_d is:

$$C_d = 312 \text{ pF}$$

Thus the element values for the filter are:

Filter Input Subsection:

$$C_{IN} = 588 \text{ pF}$$

$$R_1 = 1 \text{ k}\Omega$$

Integrator Subsection:

$$C_A = 0.1 \text{ }\mu\text{F}$$

$$R_A = 5.11 \text{ k}\Omega$$

$$R_{IA} = 5.11 \text{ k}\Omega$$

Voltage Divider Subsection:

$$C_d = 312 \text{ pF}$$

$$R_v = 2.15 \text{ k}\Omega$$

$$R_o = 453 \text{ }\Omega$$

Note, the poles P_1 and P_2 are now located at:

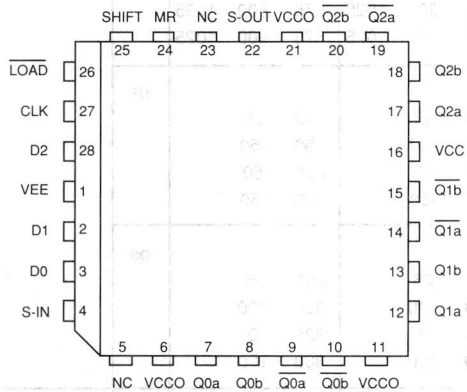
$$P_1 = -271 \text{ kHz}$$

$$P_2 = -1.36 \text{ MHz}$$

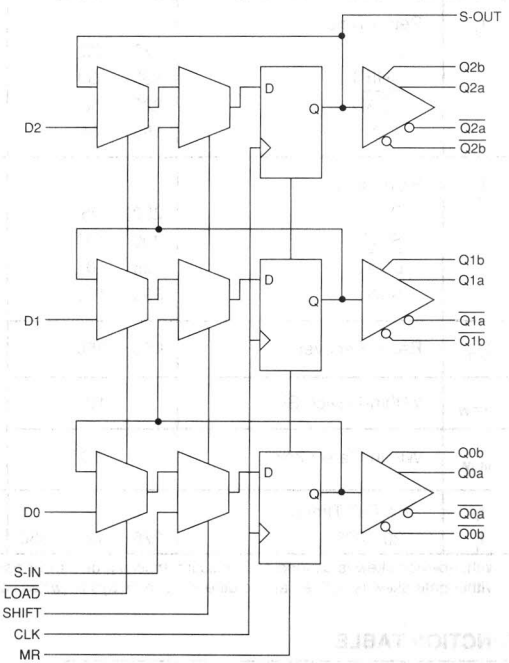
And, the open loop filter unity crossover point is at 300 kHz. As in the case of the 2:7 coding scheme, the gain can be adjusted by changing the value of R_{IA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affect the dynamic performance of the filter.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

PIN	FUNCTION
D0 – D2	Data Inputs
S-IN	Scan Input
LOAD	LOAD/HOLD Control
SHIFT	Scan Control
CLK	Clock
MR	Reset
S-OUT	Scan Output
Q[0:2]a, Q[0:2]b	True Outputs
Q[0:2]a, Q[0:2]b	Inverting Outputs

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	CLK	575	800	1025	575	800	1025	575	800	1025		
	MR	575	800	1025	575	800	1025	575	800	1025		
	CLK to S-OUT	575	800	1025	575	800	1025	575	800	1025		
t_s	Setup Time										ps	
	D	175	25		175	25		175	25			
	$\overline{SHIFT}$	150	-50		150	-50		150	-50			
	$\overline{LOAD}$	225	50		225	50		225	50			
	S-IN	150	-50		150	-50		150	-50			
t_h	Hold Time										ps	
	D	250	25		250	25		250	25			
	$\overline{SHIFT}$	300	100		300	100		300	100			
	$\overline{LOAD}$	225	0		225	0		225	0			
	S-IN	300	100		300	100		300	100			
t_{RR}	Reset Recovery	600	350		600	350		600	350		ps	
t_{SKEW}	Within-Device Skew		100			100			100		ps	1
t_{SKEW}	Within-Gate Skew		50			50			50		ps	2
t_r t_f	Rise/Fall Times 20 - 80%	275	425	650	275	425	650	275	425	650	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

FUNCTION TABLE

$\overline{LOAD}$	SHIFT	MR	MODE
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

MC10E241
MC100E241

8-BIT SCANNABLE REGISTER

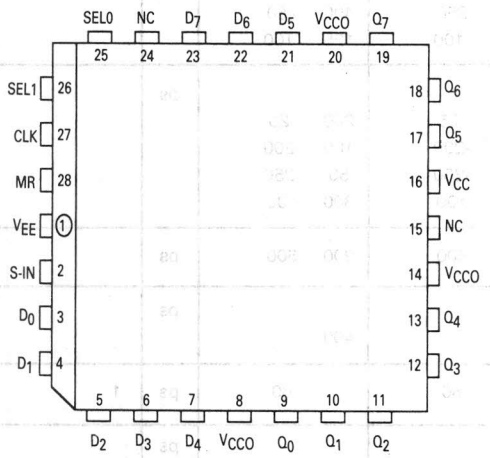
3

- SHIFT overrides HOLD/$\overline{\text{LOAD}}$ Control
- 1000 ps Max. CLK to Q
- Asynchronous Master Reset
- Pin-Compatible with E141
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

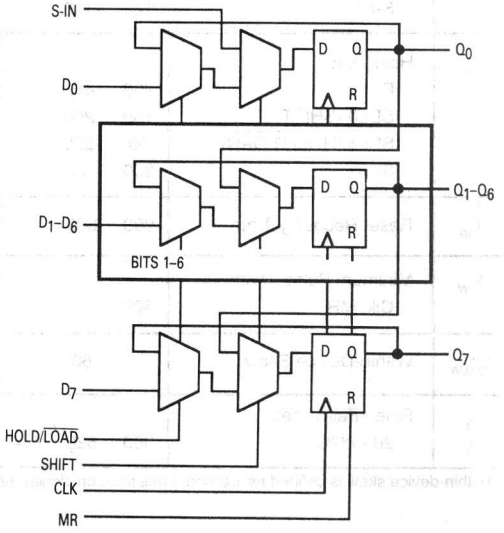
The MC10E/100E241 is an 8-bit shiftable register. Unlike a standard universal shift register such as the E141, the E241 features internal data feedback organized so that the SHIFT control overrides the HOLD/$\overline{\text{LOAD}}$ control. This enables the normal operations of HOLD and LOAD to be toggled with a single control line without the need for external gating. It also enables switching to scan mode with the single SHIFT control line.

The eight inputs D_0–D_7 accept parallel input data, while S-IN accepts serial input data when in shift mode. Data is accepted a set-up time before the positive-going edge of CLK; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0–D_7	Parallel Data Inputs
S-IN	Serial Data Input
SEL0	SHIFT Control
SEL1	HOLD/$\overline{\text{LOAD}}$ Control
CLK	Clock
MR	Master Reset
Q_0–Q_7	Data Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		125	150		125	150		125	150		
	100E		125	150		125	150		144	173		

3

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	Clk	625	750	975	625	750	975	625	750	975		
	MR	600	725	975	600	725	975	600	725	975		
t_s	Setup Time										ps	
	D	175	25		175	25		175	25			
	SEL0 (SHIFT)	350	200		350	200		350	200			
	SEL1 (HOLD/$\overline{LOAD}$)	400	250		400	250		400	250			
	S-IN	125	-100		125	-100		125	-100			
t_h	Hold Time										ps	
	D	200	-25		200	-25		200	-25			
	SEL0 (SHIFT)	100	-200		100	-200		100	-200			
	SEL1 (HOLD/$\overline{LOAD}$)	50	-250		50	-250		50	-250			
	S-IN	300	100		300	100		300	100			
t_{RR}	Reset Recovery Time	900	600		900	600		900	600		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		60			60			60		ps	1
t_r t_f	Rise / Fall Times										ps	
	20 - 80%	300	525	800	300	525	800	300	525	800		

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E256
MC100E256

**3-BIT
4:1 MUX-LATCH**

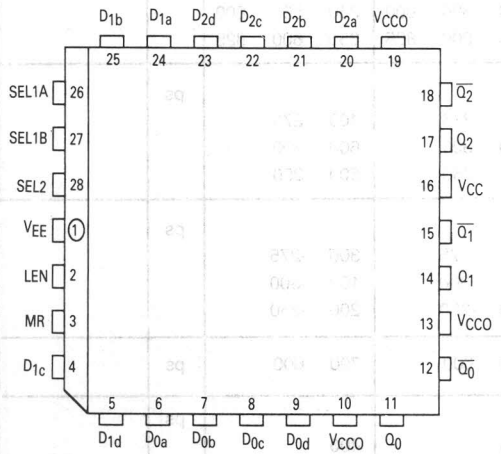
3

- 950 ps Max. D to Output
- 850 ps Max. LEN to Output
- Split Select
- Differential Outputs
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

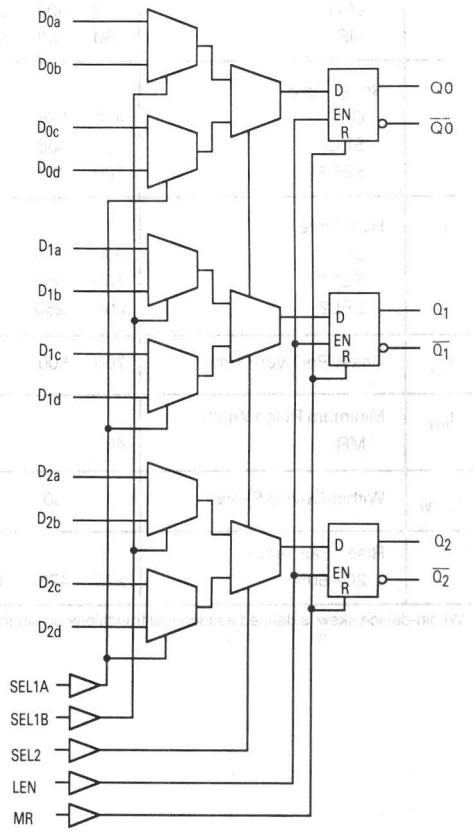
The MC10E/100E256 contains three 4:1 multiplexers followed by transparent latches with differential outputs. Separate Select controls are provided for the leading 2:1 mux pairs (see logic symbol).

When the Latch Enable (LEN) is LOW, the latch is transparent, and output data is controlled by the multiplexer select controls. A logic HIGH on LEN latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



FUNCTION TABLE

Pin	State	Operation
SEL2	H	Output c/d Data
SEL1A	H	Input d Data
SEL1B	H	Input b Data

PIN NAMES

Pin	Function
D_{0x}–D_{2x}	Data Inputs
SEL1A, SEL1B	First-stage Select Inputs
SEL2	Second-stage Select Input
LEN	Latch Enable
MR	Master Reset
Q_0, $\overline{Q_0}$–Q_2, $\overline{Q_2}$	Data Outputs

Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Note
t_{PLH} t_{PHL}	Propagation Delay to Output D SEL1 SEL2 LEN MR	 400 550 450 350 350	 600 775 650 500 600	 900 1050 900 800 825	 400 550 450 350 350	 600 775 650 500 600	 900 1050 900 800 825	 400 550 450 350 350	 600 775 650 500 600	 900 1050 900 800 825	ps	
t_s	Setup Time D SEL1 SEL2	 400 600 500	 275 300 250		 400 600 500	 275 300 250		 400 600 500	 275 300 250		ps	
t_h	Hold Time D SEL1 SEL2	 300 100 200	 -275 -300 -250		 300 100 200	 -275 -300 -250		 300 100 200	 -275 -300 -250		ps	
t_{RR}	Reset Recovery Time	700	600		700	600		700	600		ps	
t_{PW}	Minimum Pulse Width MR	 400			 400			 400			ps	
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_r t_f	Rise / Fall Times 20 - 80%	 275	 475	 700	 275	 475	 700	 275	 475	 700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device

MC10E336
MC100E336

3-BIT REGISTERED BUS TRANSCEIVER

3

- 25 Ω Cutoff Bus Outputs
- 50 Ω Receiver Outputs
- Transmit and Receive Registers
- 1500 ps Max. Clock to Bus
- 1000 ps Max. Clock to Q
- Bus Outputs Feature Internal Edge Slow-Down Capacitors
- Additional Package Ground Pins
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

The MC10E/100E336 contains three bus transceivers with both transmit and receive registers. The bus outputs ($\overline{BUS0}$–$\overline{BUS2}$) are specified for driving a 25 Ω bus; the receive outputs (Q0–Q2) are specified for 50 Ω. The bus outputs feature a normal HIGH level (V_{OH}) and a cutoff LOW level — when LOW, the outputs go to −2.0 V and the output emitter-follower is "off," presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

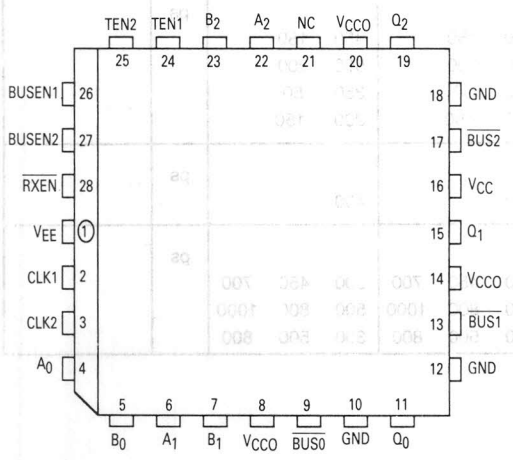
The Transmit Enable pins (TEN) control whether current data is held in the transmit register, or new data is loaded from the A/B inputs. A LOW on both of the Bus Enable inputs (BUSEN), when clocked through the register, disables the bus outputs to −2.0 V.

The receiver section clocks bus data into the receive registers, after gating with the Receive Enable ($\overline{RXEN}$) input.

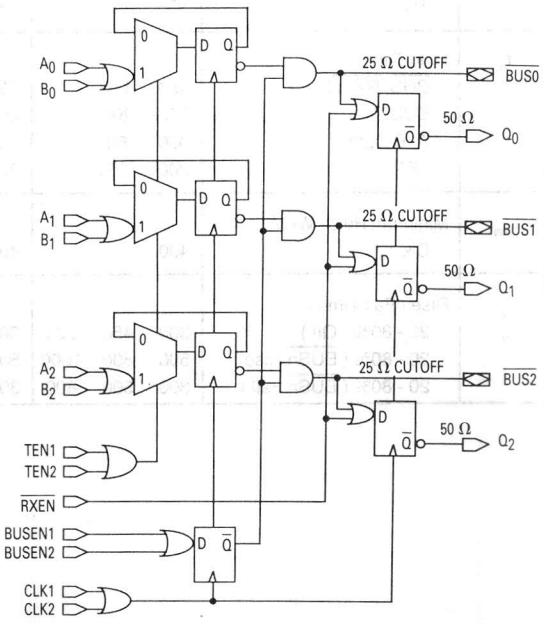
All registers are clocked by a positive transition of CLK1 or CLK2 (or both).

Additional leadframe grounding is provided through the Ground pins (GND) which should be connected to 0 V. The GND pins are not electrically connected to the chip.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
V_{CUT}	*Cut-off Output Voltage	-2.10		-2.03	-2.10		-2.03	-2.10		-2.03	V	
I_{IH}	Input HIGH Current										µA	
	$\overline{RXEN}$			225			225			225		
	All Other Inputs			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		125	150		125	150		125	150		
	100E		125	150		125	150		144	173		

*measured with V_{TT} = -2.10V

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	Clk to Q	500	700	100	500	700	1000	500	700	1000		
	Clk to $\overline{BUS}$	825	1250	1800	825	1250	1800	825	1250	1800		
t_s	Setup Time										ps	
	$\overline{BUS}$, $\overline{RXEN}$	150	-150		150	-150		150	-150			
	BUSEN	100	-200		100	-200		100	-200			
	A, B Data	300	-50		300	-50		300	-50			
	TEN	450	150		450	150		450	150			
t_h	Hold Time										ps	
	$\overline{BUS}$, $\overline{RXEN}$	450	150		450	150		450	150			
	BUSEN	500	200		500	200		500	200			
	A, B Data	350	50		350	50		350	50			
	TEN	200	-150		200	-150		200	-150			
t_{PW}	Minimum Pulse Width										ps	
	Clk	400			400			400				
t_r	Rise / Fall Times										ps	
t_f	20 - 80% (Qn)	300	450	700	300	450	700	300	450	700		
	20 - 80% ($\overline{BUS}$n Rise)	500	800	1000	500	800	1000	500	800	1000		
	20 - 80% ($\overline{BUS}$n Fall)	300	500	800	300	500	800	300	500	800		

- Bus Outputs Feature Internal Edge Slow-Down Capacitors
- Additional Package Ground Pins
- Extended 100E V_{EE} Range of −4.2 V to −5.46 V
- 75 kΩ Input Pulldown Resistors

The MC10E/100E337 is a 3-bit registered bus transceiver with scan. The bus outputs (BUS0–BUS2) are specified for driving a 25 Ω bus; the receive outputs (Q0–Q2) are specified for 50 Ω. The bus outputs feature a normal HIGH level (V_{OH}) and a cutoff LOW level — when LOW, the outputs go to −2.0 V and the output emitter-follower is "off," presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

Both drive and receive sides feature the same logic, including a loopback path to hold data. The HOLD/$\overline{\text{LOAD}}$ function is controlled by Transmit Enable (TEN) and Receive Enable (REN) on the transmit and receive sides respectively, with a HIGH selecting LOAD. Note that the implementation of the E337 Receive Enable differs from that of the E336.

A synchronous bus enable (SBUSEN) is provided for normal, non-scan operation. The asynchronous bus disable ($\overline{\text{ABUSDIS}}$) disables the bus immediately for scan mode.

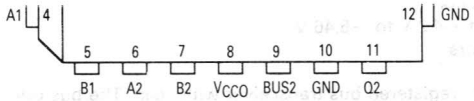
The $\overline{\text{SYNCEN}}$ input is provided for flexibility when re-enabling the bus after disabling with $\overline{\text{ABUSDIS}}$, allowing either synchronous or asynchronous re-enabling. An alternative use is asynchronous-only operation with $\overline{\text{ABUSDIS}}$, in which case $\overline{\text{SYNCEN}}$ is tied LOW, or left open. $\overline{\text{SYNCEN}}$ is implemented as an overriding SET control (active-LOW) to the enable flip-flop.

Scan mode is selected by a HIGH at the SCAN input. Scan input data is shifted in through S_IN, and output data appears at the Q2 output.

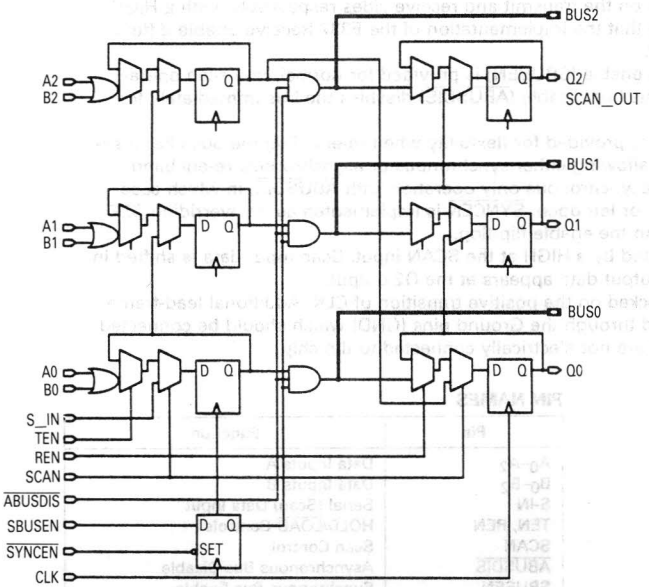
All registers are clocked on the positive transition of CLK. Additional lead-frame grounding is provided through the Ground pins (GND) which should be connected to 0 V. The GND pins are not electrically connected to the chip.

PIN NAMES

Pin	Function
A_0–A_2	Data Inputs A
B_0–B_2	Data Inputs B
S-IN	Serial (Scan) Data Input
TEN, REN	HOLD/$\overline{\text{LOAD}}$ Controls
SCAN	Scan Control
$\overline{\text{ABUSDIS}}$	Asynchronous Bus Disable
SBUSEN	Synchronous Bus Enable
$\overline{\text{SYNCEN}}$	Synchronous Enable Control
CLK	Clock
BUS0–BUS2	25 Ω Cutoff Bus Outputs
Q0–Q2	Receive Data Outputs (Q2 serves as SCAN_OUT in scan mode)



LOGIC SYMBOL



DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
V_{CUT}	*Cut-off Output Voltage	-2.10		-2.03	-2.10		-2.03	-2.10		-2.03	V	
I_{IH}	Input HIGH Current All Other Inputs			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		145	174		145	174		145	174		
	100E		145	174		145	174		167	200		

*measured with V_{TT} = -2.10V

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	Clk to Q	450		1000	450		1000	450		1000		
	Clk to BUS	800		1800	800		1800	800		1800		
	$\overline{\text{ABUSDIS}}$	500		1500	500		1500	500		1500		
	$\overline{\text{SYNCEN}}$	800		1800	800		1800	800		1800		
t_s	Setup Time										ps	
	BUS	350			350			350				
	SBUSEN	100			100			100				
	Data, S-IN	400			400			400				
	TEN, REN, SCAN	550			550			550				
t_h	Hold Time										ps	
	BUS	350			350			350				
	SBUSEN	500			500			500				
	Data, S-IN	350			350			350				
	TEN, REN, SCAN	200			200			200				
t_{PW}	Minimum Pulse Width										ps	
	Clk	400			400			400				
t_r t_f	Rise / Fall Times										ps	
	20 - 80% (Qn)	300		800	300		800	300		800		
	20 - 80% (BUSn Rise)	500		1000	500		1000	500		1000		
	20 - 80% (BUSn Fall)	300		800	300		800	300		800		

MC10E404
MC100E404

QUAD DIFFERENTIAL AND/NAND

- Differential D and Q
- 700 ps Max. Propagation Delay
- High Frequency Outputs
- Extended 100E VEE Range of -4.2V to -5.46V
- Internal 75kΩ Input Pulldown Resistors

3

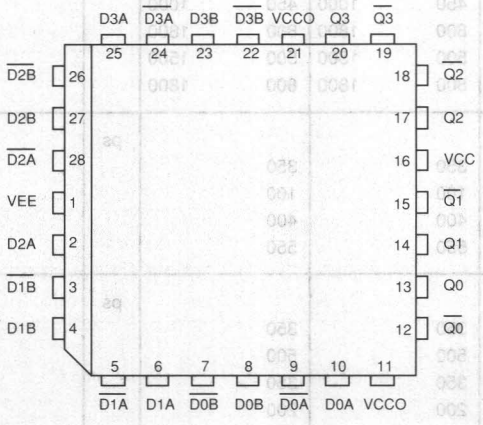
The MC 10E404/100E404 is a 4-bit differential AND/NAND device. The differential operation of the device makes it ideal for pulse shaping applications where duty cycle skew is critical. Special design techniques were incorporated to minimize the skew between the upper and lower level gate inputs.

Because a negative 2-input NAND function is equivalent to a 2-input OR function, the differential inputs and outputs of the device also allow for its use as a fully differential 2 input OR/NOR function.

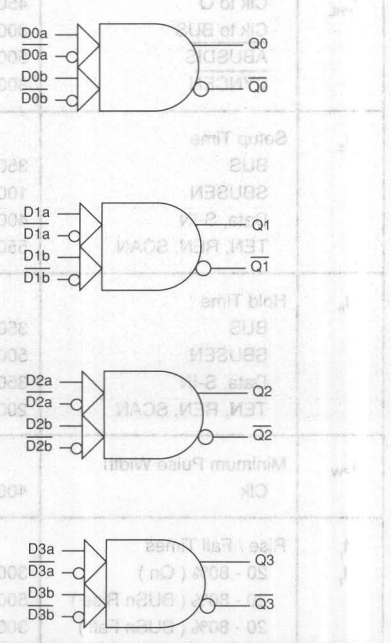
The output RISE/FALL times of this device are significantly faster than most other standard ECLinPS devices resulting in an increased bandwidth.

The differential inputs have clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus inputs of unused gates can be left open and will not affect the operation of the rest of the device.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

PIN	FUNCTION
D[0:4], $\overline{D}$[0:4]	Differential Data Inputs
Q[0:4], $\overline{Q}$[0:4]	Differential Data Outputs

FUNCTION TABLE

Da	Db	Q	$\overline{Da}$	$\overline{Db}$	$\overline{Q}$
L	L	L	L	L	L
L	H	L	L	H	H
H	L	L	H	L	H
H	H	H	H	H	H

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

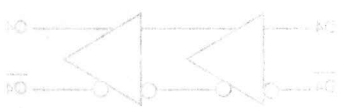
Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		106	127		106	127		106	127		
	100E		106	127		106	127		122	146		
$V_{PP}(DC)$	Input Sensitivity	50			50			50			mV	1
V_{CMR}	Common Mode Range	-1.5		0	-1.5		0	-1.5		0	V	2

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than $V_{PP\,MIN}$ and < 1V.

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	Da (Diff)	350	475	650	350	475	650	350	475	650		
	Da (SE)	300	475	700	300	475	700	300	475	700		
	Db (Diff)	375	500	675	375	500	675	375	500	675		
	Db (SE)	325	500	725	325	500	725	325	500	725		
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
$V_{PP}(AC)$	Minimum Input Swing	150			150			150			mV	2
t_r t_f	Rise / Fall Time 20 - 80%	150		400	150		400	150		400	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Minimum input swing for which AC parameters are guaranteed.



MC10E416
MC100E416

QUINT DIFFERENTIAL LINE RECEIVER

- Differential D and Q; V_{BB} available
- 600 ps Max. Propagation Delay
- High Frequency Outputs
- 2 Stages of Gain
- Extended 100E VEE Range of -4.2V to -5.46V
- Internal 75kΩ Input Pulldown Resistors

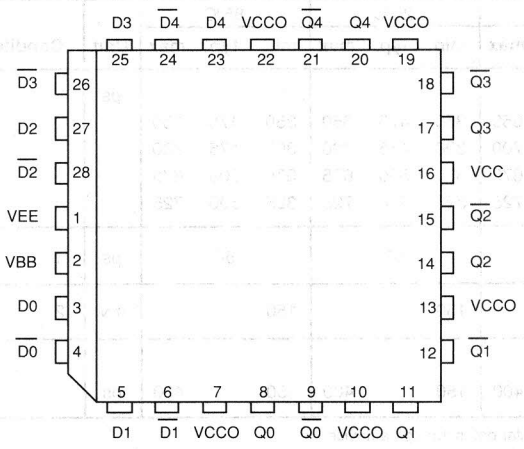
3

The MC 10E416/100E416 is a 5-bit differential line receiving device. The 2.0 GHz of bandwidth provided by the high frequency outputs makes the device ideal for buffering of very high speed oscillators.

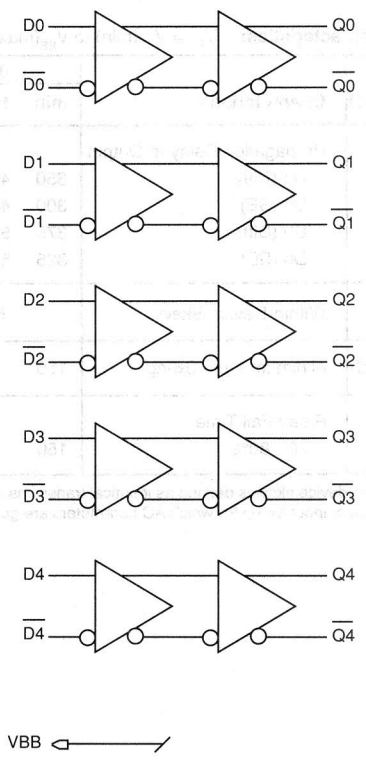
A V_{BB} pin is available to AC couple an input signal to the device. More information on AC coupling can be found in the design handbook section of this data book.

The design incorporates two stages of gain internal to the device making it an excellent choice for use in high bandwidth amplifier applications.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

PIN	FUNCTION
D[0:4], $\overline{D}$[0:4]	Differential Data Inputs
Q[0:4], $\overline{Q}$[0:4]	Differential Data Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

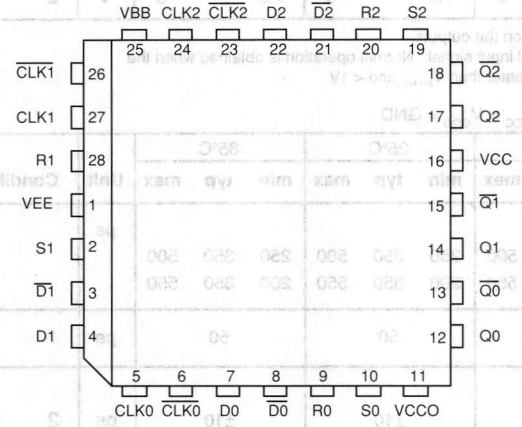
Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
V_{BB}	Output Reference Voltage										V	
	10E	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19		
	100E	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		135	162		135	162		135	162		
	100E		135	162		135	162		155	186		
$V_{PP}(DC)$	Input Sensitivity	50			50			50			mV	1
V_{CMR}	Common Mode Range	-1.5		0	-1.5		0	-1.5		0	V	2

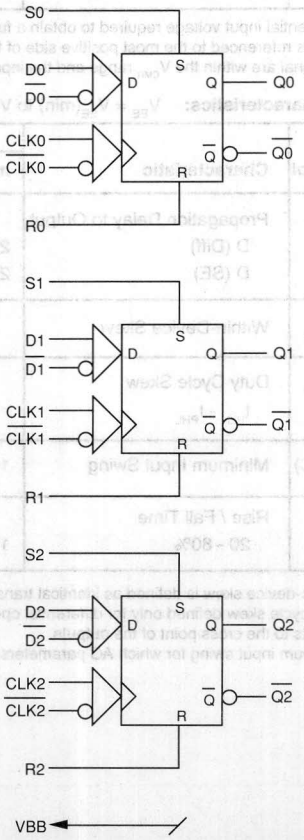
1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signal are within the V_{CMR} range and the input swing is greater than $V_{PP\ MIN}$ and < 1V

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D (Diff)	250	350	500	250	350	500	250	350	500		
	D (SE)	200	350	550	200	350	550	200	350	550		
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_{SKEW}	Duty Cycle Skew											
	$t_{PLH} - t_{PHL}$		±10			±10			±10		ps	2
$V_{pp}(AC)$	Minimum Input Swing	150			150			150			mV	3
t_r	Rise / Fall Time											
t_f	20 - 80%	100	200	350	100	200	350	100	200	350	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device
2. Duty cycle skew defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. Minimum input swing for which AC parameters are guaranteed





PIN NAMES

PIN	FUNCTION
D[0:2], $\overline{D}$[0:2]	Differential Data Inputs
CLK[0:2], $\overline{CLK}$[0:2]	Differential Clock Inputs
S[0:2]	Edge Triggered Set Inputs
R[0:2]	Edge Triggered Reset Inputs
VBB	VBB Reference Output
Q[0:2], $\overline{Q}$[0:2]	Differential Data Outputs

FUNCTION TABLE

Dn	CLKn	Rn	Sn	Qn
L	Z	L	L	L
H	Z	L	L	H
X	L	Z	L	L
X	L	L	Z	H

Z=Low to high transition

V_{CMR}	Common Mode Range	-1.5		0	-1.5		0	-1.5		0	V	1

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal specified operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than $V_{PP\ MIN}$ and < 1V.

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
f_{MAX}	Max. Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	CLK (Diff)	450	600	750	450	600	750	450	600	750		
	CLK (SE)	400	600	800	400	600	800	400	600	800		
	R	550	725	925	550	725	925	550	725	925		
	S	550	725	925	550	725	925	550	725	925		
t_s	Setup Time										ps	
	D	200	0		200	0		200	0			
	R	1000	700		1000	700		1000	700			1
	S	1000	700		1000	700		1000	700			1
t_h	Hold Time										ps	
	D	200	0		200	0		200	0			
t_{PW}	Minimum Pulse Width										ps	
	CLK	400			400			400				
t_{SKEW}	Within-Device Skew		50			50			50		ps	2
$V_{PP}(AC)$	Minimum Input Swing	150			150			150			mV	3
t_r t_f	Rise/Fall Times										ps	
	20 - 80%	275	450	650	275	450	650	275	450	650		

1. These setup times define the minimum time the CLK or SET/RESET input must wait after the assertion of the RESET/SET input to assure the proper operation of the flip-flop.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Minimum input swing for which AC parameters are guaranteed.

Product Preview

MC10E445
MC100E445

4-BIT SERIAL/PARALLEL CONVERTER

- On Chip Clock ÷4 and ÷8
- 2.5Gb/s Data Rate Capability
- Differential Clock and Serial Inputs
- VBB Output for Single-ended Input Applications
- Asynchronous Data Synchronization
- Mode Select to Expand to 8 Bits
- Internal 75kΩ Input Pulldown Resistors
- Extended 100E VEE Range of -4.2V to -5.46V

3

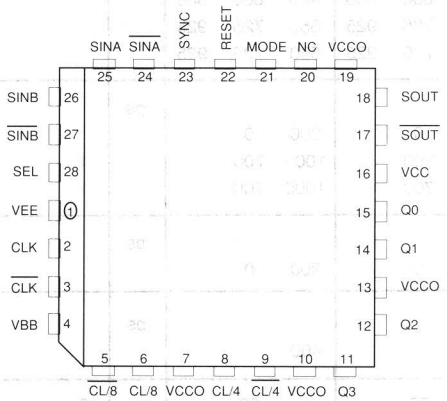
The MC10E/100E445 is an integrated 4-bit serial to parallel data converter. The device is designed to operate for NRZ data rates of up to 2.5Gb/s. The chip generates a divide by four and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the first serial bit to Q0, the second to Q1 etc.

Two selectable serial inputs provide a loopback capability for testing purposes when the device is used in conjunction with the E446 parallel to serial converter.

The start bit for conversion can be moved using the SYNC input. A single pulse applied asynchronously for at least two cycles of the input clock signal shifts the start bit for conversion by one bit. For each additional shift required, an additional pulse must be supplied.

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. When the MODE input is driven HIGH the data at the output will change on every eighth clock cycle thus allowing for an 8-bit conversion scheme using two E445's.

PINOUT: 28-LEAD PLCC (TOP VIEW)



PIN NAMES

PIN	FUNCTION
SINA, SINA	Diff. Serial Data Input A
SINB, SINB	Diff. Serial Data Input B
SEL	Serial Input Select Pin
SOUT, SOUT	Diff. Serial Data Output
Q0-Q3	Parallel Data Outputs
CLK, CLK	Diff. Clock Inputs
CL/4, CL/4	Diff. ÷4 Clock Output
CL/8, CL/8	Diff. ÷8 Clock Output
MODE	Conversion Mode 4-bit/8-bit
SYNCH	Conversion Synchronizing Input

FUNCTION TABLES

MODE	Conversion
L	4 Bit
H	8 Bit

SEL	Serial Input
H	A
L	B

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC10E446
MC100E446

4-BIT PARALLEL/SERIAL CONVERTER

3

Product Preview

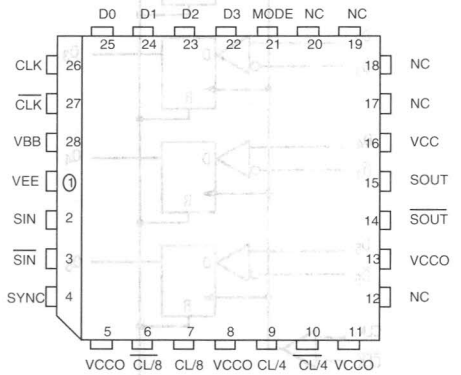
- On Chip Clock ÷4 and ÷8
- 2.5Gb/s Data Rate Capability
- Differential Clock and Serial Inputs
- VBB Output for Single-ended Input Applications
- Mode Select to Expand to 8 Bits
- Internal 75kΩ Input Pulldown Resistors
- Extended 100E VEE Range of -4.2V to -5.46V

The MC10E/100E446 is an integrated 4-bit parallel to serial data converter. The device is designed to operate for NRZ data rates of up to 2.5Gb/s. The chip generates a divide by four and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the parallel data into a serial stream from bit D0 to D3. A serial input is provided to cascade two E446 devices for 8 bit conversion applications.

The SYNC input can be used to reset the internal clock conversion unit to select the start of the conversion process.

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. With the MODE input driven HIGH data at the serial input are read at one half of the ÷8 clock cycle thus allowing for an 8 bit conversion using two E446's.

PINOUT: 28-LEAD PLCC (TOP VIEW)



PIN NAMES

PIN	FUNCTION
SIN	Diff. Serial Data Input
D0-D3	Parallel Data Input
SOUT, $\overline{\text{SOUT}}$	Diff. Serial Data Output
CLK, $\overline{\text{CLK}}$	Diff. Clock Input
CL/4, $\overline{\text{CL/4}}$	Diff. 4 Clock Output
CL/8, $\overline{\text{CL/8}}$	Diff. 8 Clock Output
MODE	Conversion Mode, 4 bit/8 bit
SYNC	Conversion Synchronizing Input

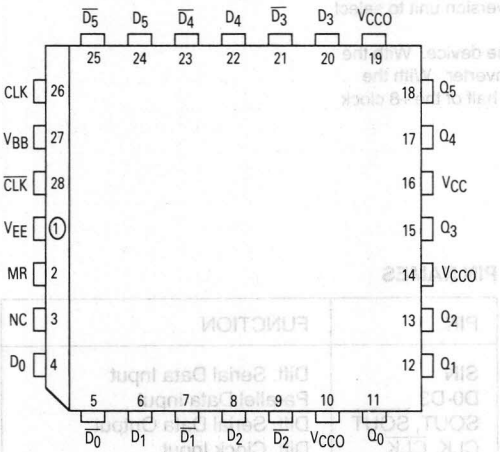
FUNCTION TABLES

MODE	Conversion
L	4 Bit
H	8 Bit

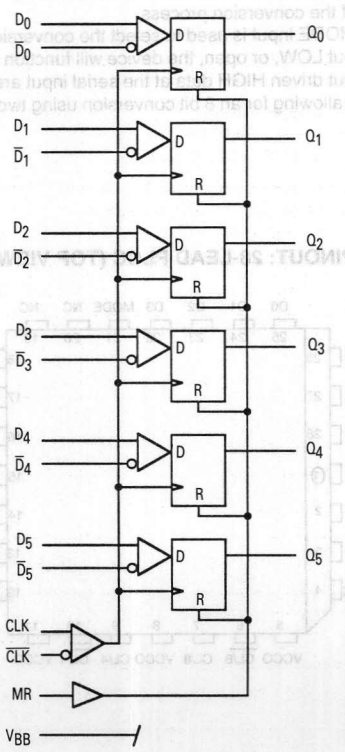
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 μF capacitor.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_0–D_5	+ Data Input
$\overline{D_0}$–$\overline{D_5}$	– Data Input
CLK	+ Clock Input
$\overline{CLK}$	– Clock Input
MR	Master Reset Input
V_{BB}	V_{BB} Output
Q_0–Q_5	Data Outputs

VCMR	Common Mode Range	-2.0		-0.4	-2.0		-0.4	-2.0	-0.4	V	2

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than V_{PPMIN} and < 1V.

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
f_{MAX}	Max. Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output CLK (Diff) CLK (SE) MR	 475 425 425	 650 650 600	 800 850 850	 475 425 425	 650 650 600	 800 850 850	 475 425 425	 650 650 600	 800 850 850	ps	
t_s	Setup Time D	 150	 -100		 150	 -100		 150	 -100		ps	
t_h	Hold Time D	 250	 100		 250	 100		 250	 100		ps	
$V_{PP}(AC)$	Minimum Input Swing	150			150			159			mV	1
t_{RR}	Reset Recovery Time	750	600		750	600		750	600		ps	
t_{PW}	Minimum Pulse Width CLK, MR	 400			 400			 400			ps	
t_{SKEW}	Within-Device Skew		100			100			100		ps	2
t_r t_f	Rise / Fall Times 20 - 80%	 275	 450	 800	 275	 450	 800	 275	 450	 800	ps	

1. Minimum input voltage for which AC parameters are guaranteed
2. Within-device skew is defined as identical transitions on similar paths through a device

MC10E452
MC100E452

5-BIT DIFFERENTIAL REGISTER

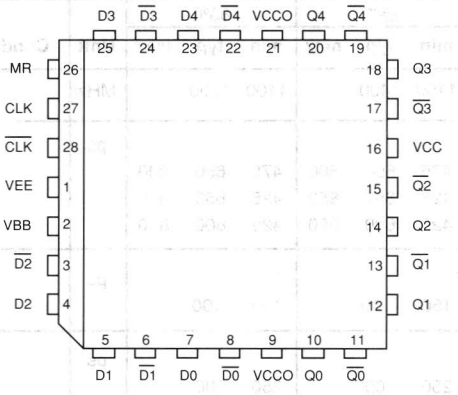
- Differential D, CLK and Q; VBB Reference Available
- 1100 MHz Min. Toggle Frequency
- Asynchronous Master Reset
- Extended 100E VEE Range of -4.2V to -5.46V

The MC 10E/100E452 is a 5-bit differential register with differential data (inputs and outputs) and clock. The registers are triggered by a positive transition of the positive clock (CLK) input. A high on the Master Reset (MR) asynchronously resets all registers so that the Q outputs go LOW.

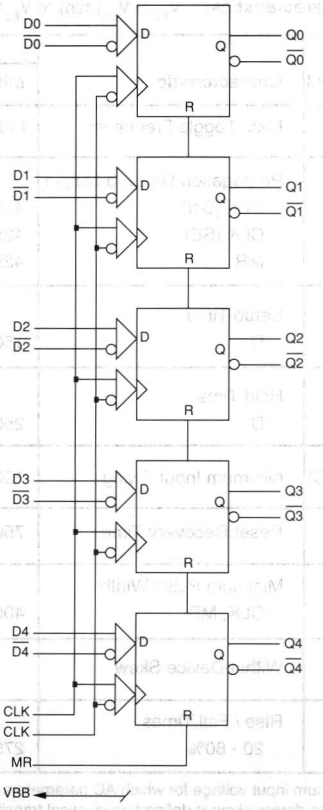
The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge triggered flip flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state.

The fully differential design of the device makes it ideal for very high frequency applications where a registered data path is necessary.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

PIN	FUNCTION
D[0:4], $\overline{D}$[0:4]	Differential Data Inputs
MR	Master Reset Input
CLK, $\overline{CLK}$	Differential Clock Input
VBB	VBB Reference Output
Q[0:4], $\overline{Q}$[0:4]	Differential Data Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
V_{BB}	Output Reference Voltage										V	
	10E	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19		
	100E	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		74	89		74	89		74	89		
	100E		74	89		74	89		85	102		
V_{CMR}	Common Mode Range	-2.0		-0.4	-2.0		-0.4	-2.0		-0.4	V	1

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signal are within the V_{CMR} range and the input swing is greater than $V_{PP\,MIN}$ and < 1V.

AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C min	0°C typ	0°C max	25°C min	25°C typ	25°C max	85°C min	85°C typ	85°C max	Unit	Condition
f_{MAX}	Max. Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	CLK (Diff)	475	600	800	475	600	800	475	600	800		
	CLK (SE)	425	600	850	425	600	850	425	600	850		
	MR	425	625	850	425	625	850	425	625	850		
t_s	Setup Time										ps	
	D	150	-50		150	-50		150	-50			
t_h	Hold Time										ps	
	D	200	50		200	50		200	50			
t_{RR}	Reset Recovery Time	700	450		700	450		700	450		ps	
t_{PW}	Minimum Pulse Width										ps	
	CLK	400			400			400				
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
$V_{PP}(AC)$	Minimum Input Swing	150			150			150			mV	2
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	475	675	275	475	675	275	475	675		

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Minimum input swing for which AC parameters are guaranteed.

MC10E457
MC100E457

TRIPLE DIFFERENTIAL 2:1 MULTIPLEXER

- Differential D and Q; V_{BB} available
- 700 ps Max. Propagation Delay
- High Frequency Outputs
- Separate and Common Select
- Extended 100E VEE Range of -4.2V to -5.46V
- Internal 75kΩ Input Pulldown Resistors

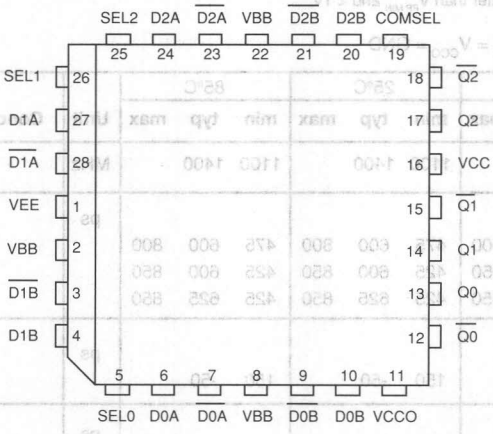
3

The MC 10E457/100E457 is a 3-bit differential 2:1 multiplexer. The fully differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple VBB pins are provided to ease AC coupling input signals.

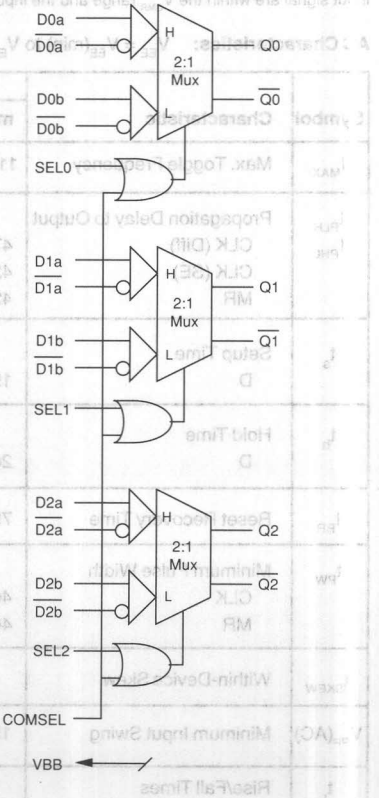
The higher frequency outputs provide the device with a >1.0 GHz bandwidth to meet the needs of the most demanding system clock.

Both separate selects and a common select are provided to make the device well suited for both data path and random logic applications.

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



FUNCTION TABLE

SEL	Data
H	a
L	b

PIN NAMES

PIN	FUNCTION
Dn[0:2], $\overline{Dn}$[0:2]	Differential Data Inputs
SEL	Individual Select Input
COMSEL	Common Select Input
VBB	VBB Reference Output
Q[0:2], $\overline{Q}$[0:2]	Differential Data Outputs

DC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
V_{BB}	Output Reference Voltage										V	
	10E	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19		
	100E	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		92	110		92	110		92	110		
	100E		92	110		92	110		106	127		
$V_{PP}(DC)$	Input Sensitivity	50			50			50			mV	1
V_{CMR}	Common Mode Range	-1.5		0	-1.5		0	-1.5		0	V	2

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signal are within the V_{CMR} range and the input swing is greater than $V_{PP\,MIN}$ and < 1V.

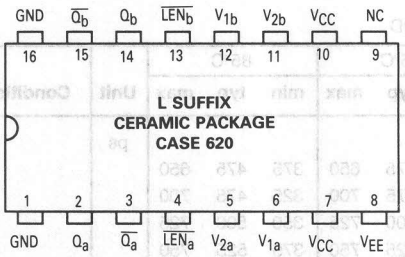
AC Characteristics: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$

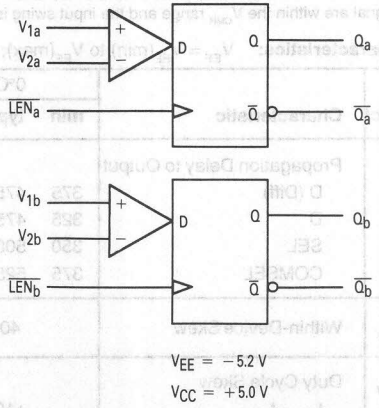
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D (Diff)	375	475	650	375	475	650	375	475	650		
	D	325	475	700	325	475	700	325	475	700		
	SEL	350	500	725	350	500	725	350	500	725		
	COMSEL	375	525	750	375	525	750	375	525	750		
t_{SKEW}	Within-Device Skew		40			40			40		ps	1
t_{SKEW}	Duty Cycle Skew											
	$t_{PLH} - t_{PHL}$		±10			±10			±10		ps	2
$V_{PP}(AC)$	Minimum Input Swing	150			150			150			mV	3
t_r	Rise / Fall Time											
t_f	20 - 80%	150	275	450	150	275	450	150	275	450	ps	

1. Within-device skew is guaranteed for identical transitions on similar paths through a device
2. Duty cycle skew guarantee holds only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. Minimum Input Swing for which AC parameters are guaranteed.

the MECL III family, but is fabricated on Motorola's advanced MOSAIC III process. The part has been designed with the goal of minimizing variations in propagation delay versus the amount of input overdrive. The output voltage levels are compatible with 10KH (and 10E) standard logic devices.

PINOUT: 16-PIN CERAMIC DIP (TOP VIEW)





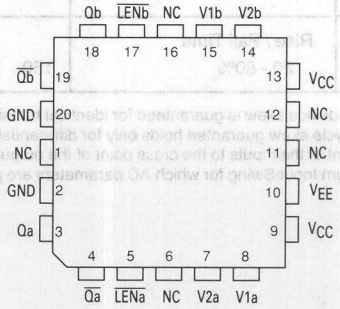
V_{EE} = −5.2 V

V_{CC} = +5.0 V

FUNCTION TABLE

$\overline{LEN}$	V1, V2	Q
H	V1 > V2	H
H	V1 < V2	L
L	X	Latched

10E1651 20-LEAD PLCC PINOUTS



This document contains information on a new product. Specifications and information are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS:
Beyond which device life may be impaired

Symbol	Characteristic	min	typ	max	Unit
VSUP	Total Supply Voltage |VEE| + |VCC|			12.0	V
VPP	Differential Input Voltage |V1 - V2|			3.0	V

DC Characteristics: V_{EE} = -5.2 V ± 5%; V_{CC} = +5.0V ± 5%

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
V_{OH}	Ouput HIGH Voltage	-1020		-840	-980		-810	-920		-735	mV	
V_{OL}	Output Low Voltage	-1950		-1630	-1950		-1630	-1950		-1600	mV	
II I_{IH}	Input Current (V1, V2) Input HIGH Current (LEN)			65 150			65 150			65 150	µA	
I_{CC} I_{EE}	Positive Supply Current Negative Supply Current			50 -55			50 -55			50 -55	mA	
VCMR	Common Mode Range	-2.0		3.0	-2.0		3.0	-2.0		3.0	V	

AC Characteristics: V_{EE} = -5.2 V ± 5%; V_{CC} = +5.0V ± 5%

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output $\overline{V}$ to Q $\overline{LEN}$ to Q	 600 500	 850 750	 1150 950	 600 500	 850 750	 1150 950	 600 500	 850 750	 1150 950	ps	
t_r t_f	Rise / Fall Times 20 - 80%	 200	 300	 700	 200	 300	 700	 200	 300	 700	ps	

Note: Contact factory for more complete data sheet

MC10E1652

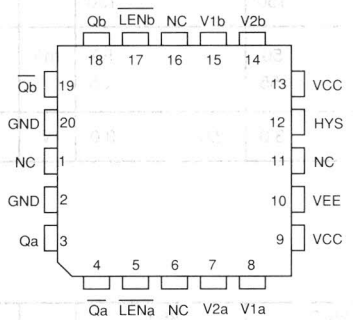
DUAL ANALOG COMPARATOR w/ LATCH

- Typ. 3.0 dB Bandwidth > 1.0GHz
- Typ. V to Q Propagation Delay of 850 ps
- Typ. Output Rise/Fall of 300 ps
- Common Mode Range -2.0 V to +3.0 V
- Individual Latch Enables
- Differential Outputs
- User Controlled Input Hysterisis

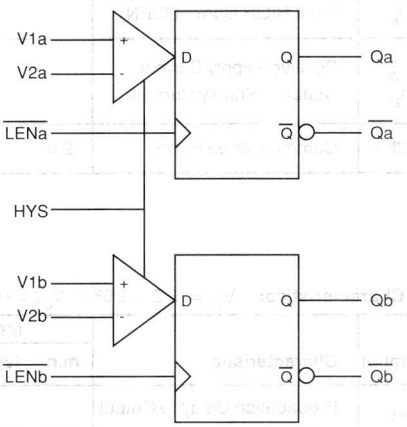
3

The MC10E1652 is functionally compatible with the MC10E1651 and thus the MC1651 in the MECL III family. The hysterisis control pin HYS allows the user to define the amount of input hysterisis where as the MC10E1651 has a built in fixed level of input hysterisis. The device comes in a 10E version only, thus the outputs are only compatible with 10KH logic devices. The device is available in both a 16-pin DIP and a 20-pin PLCC surface mount package.

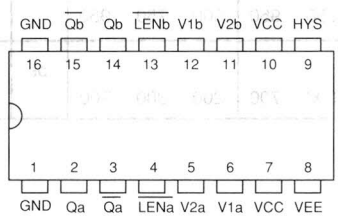
PINOUT: 20-LEAD PLCC (TOP VIEW)



LOGIC DIAGRAM



PINOUT: 16-PIN CERAMIC DIP (TOP VIEW)



FUNCTION TABLE

$\overline{LEN}$	V1, V2	Q
H	V1 > V2	H
H	V1 < V2	L
L	X	Latched

ABSOLUTE MAXIMUM RATINGS:
Beyond which device life may be impaired

Symbol	Characteristic	min	typ	max	Unit
VSUP	Total Supply Voltage |VEEI + |VCCI			12.0	V
VPP	Differential Input Voltage |V1 - V2|			3.0	V

DC Characteristics: V_{EE} = -5.2 V ± 5%; V_{CC} = +5.0V ± 5%

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
V_{OH}	Ouput HIGH Voltage	-1020		-840	-980		-810	-920		-735	mV	
V_{OL}	Output Low Voltage	-1950		-1630	-1950		-1630	-1950		-1600	mV	
II I_{IH}	Input Current (V1, V2) Input HIGH Current ($\overline{LEN}$)			65 150			65 150			65 150	µA	
I_{CC} I_{EE}	Positive Supply Current Negative Supply Current			50 -55			50 -55			50 -55	mA	
VCMR	Common Mode Range	-2.0		3.0	-2.0		3.0	-2.0		3.0	V	

AC Characteristics: V_{EE} = -5.2 V ± 5%; V_{CC} = +5.0V ± 5%

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output $\overline{V}$ to Q $\overline{LEN}$ to Q	 600 500	 850 750	 1150 950	 600 500	 850 750	 1150 950	 600 500	 850 750	 1150 950	ps	
t_r t_f	Rise / Fall Times 20 - 80%	 200	 300	 700	 200	 300	 700	 200	 300	 700	ps	

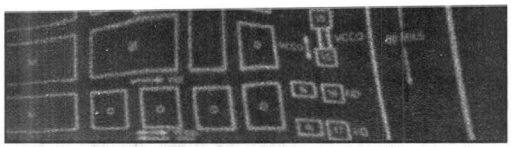
Note: Contact factory for more complete data sheet.

V_{OH}	Output HIGH Voltage	-1020	-840	-980 -810	-920 -735	mV
V_{OL}	Output Low Voltage	-1360	-1580	-1580 -1830	-1570 -1800	mV
I_{IL} I_{IH}	Input Current (V1, V2) Input HIGH Current (LEN)		65 150		65 150	µA
I_{CC} I_{EE}	Positive Supply Current Negative Supply Current		60 -55		60 -55	mA
VCMR	Common Mode Range	-2.0	3.0	-2.0 3.0	-2.0 3.0	V

AC Characteristics: V_{EE} = -5.2 V ± 5%; V_{CC} = +5.0V ± 5%

		0°C			25°C			85°C			
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output V to Q LEN to Q	800 600	980 750	1150 980	900 800	1050 750	1150 980	900 800	950 750	1150 980	ps	
t_r t_f	Rise / Fall Times 20 - 80%	200	500	700	200	500	700	200	500	700	ps	

* Note: Contact factory for more complete data sheet.



Design Guide 4

This section contains a design guide written exclusively with the ECLinPS product family in mind. The design guide deals with system design aspects of using the family. This section is not meant to be a replacement for the MECL System Design Handbook but rather a supplement to the information contained in it.

CONTENTS

SECTION 1
System Basics

Power Supply Considerations

The following text gives a brief description of the requirements and recommendation for treatment of power supplies in an ECLinPS system design. A more thorough narration on the general subject of power supplies can be found in the Motorola System Design Handbook.

V_{CC} Supply

As with all previous ECL families the ECLinPS logic family is designed to operate with negative power supplies, in other words with V_{CC} connected to ground. However ECLinPS circuits will work fine with positive power supplies as long as special care has been taken to ensure a stable, quiet V_{CC} supply. The output voltage levels for a positive supply system can be determined by simply subtracting the absolute value of the standard negative output levels from the desired V_{CC}.

To provide as small an AC impedance as possible, and minimize power bus IR drops, the V_{CC} supply should have a dedicated power plane. By providing a full ground plane in the system the designer ensures that the current return path for the signal traveling down a transmission line does not encounter any major obstructions. It is imperative that the noise and voltage drops be as small as possible on the V_{CC} plane as the internal switching references and output levels are all derived off of the V_{CC} power rail. Thus any perturbations on this rail could adversely affect the noise margins of a system.

V_{EE} Supply

To take advantage of increased logic density and temperature compensated outputs many designers are building array options with both temperature compensated output levels and a -5.2V V_{EE} supply. To alleviate any problems with interfacing these arrays to ECLinPS 100E devices Motorola has specified the operation of 100E devices to include the standard 10KH V_{EE} voltage range. Moreover, because of the superior voltage compensation of the bias network, this guarantee comes without any changes in the DC or AC specification limits. With the availability of both 10KH and 100K compatible devices in the ECLinPS family there is generally no need to run 10E devices at 100K voltage levels. If however this is desired, the 10E devices will function at100E V_{EE} levels with, at worst, a small degradation in AC performance for a few devices due to soft saturation of the current source device.

Although both the 10E and 100E devices can tolerate variations in the V_{EE} supply without any detrimental effects, it is recommended that the V_{EE} supply also have a dedicated power plane. If this is not a feasible constraint care should be taken so that the IR drops of the V_{EE} bus do not create a V_{EE} voltage outside of the specification range. To provide the switching currents resulting from stray capacitances and asymmetric loading, the V_{EE} power supply in an ECL system needs to be bypassed. It is recommended that the V_{EE} supply be bypassed at each device with an RF quality .01µF capacitor to ground. In addition the supply should also be bypassed to ground with a 1µF - 10µF capacitor at the power inputs to a board. If a separate output termination plane is used the V_{EE} supply will be of a static nature as the output switching current will return to ground via the V_{TT} supply, thus the bypassing of every device may be on the conservative side. If the design is going to include a liberal use of serial or Thevenin equivalent termination schemes a properly bypassed V_{EE} plane is essential.

V_{TT} Supply

The output edge rates of the ECLinPS family necessitate an almost exclusive use of controlled impedance transmission lines for system interconnect (the details of this claim will be discussed in a latter section). Thus, unless Thevenin equivalent termination schemes are going to be used, a V_{TT} supply is a must in ECLinPS designs. The choice of using only Thevenin equivalent termination schemes to save a power supply should not be made lightly as the Thevenin scheme consumes up to ten times more power than the equivalent parallel termination to a -2.0V V_{TT} supply.

As was the case for the V_{EE} supply, a dedicated power plane, liberally bypassed as described above, should be used for the V_{TT} supply. In designs which rely heavily on parallel termination schemes the V_{TT} supply will be responsible for returning the switching current of the outputs to ground, therefore a low AC impedance is a must. For bypassing, many SIP resistor packs have bypass capacitors integrated in their design to supply the necessary bypassing of the supply. The use of SIP resistors will be discussed more thoroughly in a latter chapter.

Handling of Unused Inputs and Outputs

Unused Inputs

All ECLinPS devices have internal 50KΩ-75KΩ pull-down resistors connected to V_{EE}. As a result an input which

is left open will be pulled to V_{EE} and thus set at a logic LOW. These internal pulldowns provide more than enough noise margin to keep the input from turning on if noise is coupled to the input, therefore there is no need to tie the inputs to V_{EE} external to the package. In addition by shorting the inputs to V_{EE} external to the package one removes the current limiting effect of the pulldown resistor and under extreme V_{EE} conditions the input transistor could be permanently damaged. If there are concerns about leaving sensitive inputs, such as clocks, open they should be tied low via an unused output or a quiet connection to V_{TT}.

Unless otherwise noted on the data sheets, the outputs to differential input devices will go to a defined state when the inputs are left open. This is accomplished via an internal clamp. Note that this clamp will only take over if the voltage at the inputs fall below ≈ -2.5V. Therefore if equal voltages of greater than -2.5V are placed on the inputs the outputs will attain an undefined midswing state.

Unlike saturating logic families the inputs to an ECLinPS, or any ECL device, cannot be tied directly to V_{CC} to implement a logic HIGH level. Tying inputs to V_{CC} will saturate the input transistor and the AC and DC performance will be seriously impaired. A logic HIGH on an ECLinPS input should be tied to a level no higher than 600mV below the V_{CC} rail and more typically no higher than the specified V_{IH}max limit. A resistor or diode tree can be used to generate a logic HIGH level or more commonly an output of an unused gate can be used.

Unused Outputs

The handling of unused outputs is guided by two criteria: power dissipation and noise generation. For single ended output devices it is highly recommended to leave unused outputs unterminated as there are no benefits in the alternative scheme. This not only saves the power associated with the output but also reduces the noise on the V_{CC} line by reducing the current being switched through the inductance of the V_{CC} pins. For the counters and shift registers of the family the count and shift frequencies will be maximized if the parallel outputs are left unterminated. Of course for applications where these parallel outputs are needed this is not a viable alternative.

For the differential outputs, on the other hand, things are a little less cut and dry. If either of the outputs of a complimentary output pair is being used both outputs of the pair should be terminated. This termination scheme minimizes the current being switched through the V_{CC} pin and thus minimizes the noise generated on V_{CC}. If, however, neither of the outputs of a complimentary pair are being used it makes most sense to leave these unterminated to save power. Note that the E111 device has special termination rules; these rules are outlined on the data sheet for the device.

Minimizing Simultaneous Switching Noise

A common occurrence among ECL families is the generation of crosstalk and other noise phenomena during simultaneous switching situations. Although the noise generated in ECL systems is minor compared to other technologies there are methods to even further minimize the problem.

Figure 1.1 below illustrates the two output scenarios of an ECL device: differential outputs and single ended outputs. During switching the current in the output device will change by ≈17mA when loaded in the normal 50Ω to -2.0V load. With differential outputs as one output switches from a low to a high state the other switches from a high to a low state simultaneously thus the resultant current change through the V_{CCO} connection is zero. The current simply switches between the two outputs. However for the single ended output, the current change flows through the V_{CCO} connection of the output device. This current change through the V_{CCO} pin of the package causes a voltage spike due to the inductance of the pin.

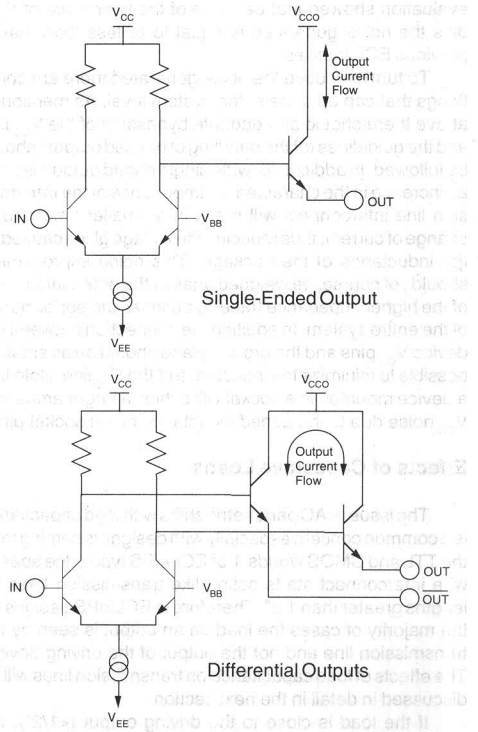


Figure 1.1 - ECL Output Structures

Traditionally manufacturers of ECL products have attempted to combat this problem by providing a separate V_{CC} pin for the output device (V_{CCO}, V_{CCA} etc.) and the internal circuitry. By doing this the noise generated on the V_{CCO} of the output devices would see a high impedance internal to the

parasitics of the package and the output device would combine to produce an instability which resulted in the outputs going into an oscillatory state. To alleviate this oscillation problem it was necessary to make the V_{CC} and V_{CCO} metal common internal to the package. Subsequent evaluation showed that because of the liberal use of V_{CCO} pins the noise generated is equal to or less than that of previous ECL families.

To further reduce the noise generated there are some things that can be done at the system level. As mentioned above there should be adequate bypassing of the V_{CC} line and the guidelines for the handling of unused outputs should be followed. In addition for wide single ended output devices an increase in the characteristic impedance of the transmission line interconnect will result in a smaller time rate of change of current; thus reducing the voltage glitch caused by the inductance of the package. This noise improvement should , of course, be weighed against the potential slowing of the higher impedance trace to optimize the performance of the entire system. In addition the connection between the device V_{CC} pins and the ground plane should be as small as possible to minimize the inductance of the V_{CC} line. Note that a device mounted in a socket will exhibit a larger amount of V_{CC} noise due to the added inductance of the socket pins.

Effects of Capacitive Loads

The issue of AC parametric shifts with load capacitance is a common concern especially with designers coming from the TTL and CMOS worlds. For ECLinPS type edge speeds wire interconnect starts acting like transmission lines for lengths greater than 1/2". Therefore in ECLinPS designs for the majority of cases the load on an output is seen by the transmission line and not the output of the driving device. The effects of load capacitance on transmission lines will be discussed in detail in the next section.

If the load is close to the driving output (<1/2"), the resulting degradation will be 15-25ps/pF for both propagation delays and edge rates. In general a capacitive load on an emitter follower has a greater impact on the falling edge than the rising edge. Therefore the upper end of the range given above represents the effect on fall times and the associated propagation delays while the lower end represents the effect on the rising output parameters.

popular way to reduce total part count and optimize the speed performance of a system. The limitation of OR-tying ECL outputs has always been a combination of increased delay per OR-tie and the negative going disturbance seen at the output when one output switches from a high to a low while the rest of the outputs remain high. For high speed devices the latter problem is the primary limitation due to the increased sensitivity to this phenomena with decreasing output transition times. The following paragraph will attempt to describe the wire-OR glitch phenomena from a physical perspective.

Figure 1.2 illustrates a typical wire-OR situation. For simplicity the discussion will deal with only two outputs, however the argument could easily be expanded to include any number of outputs. If both the A and the B outputs start in the high state they will both supply equal amounts of current to the load. If the B output then transitions from a high to a low the line at the emitter of B will see a sudden decrease in the line voltage. This negative going transition on the line will continue downward at the natural fall time of the output until the A output responds to the voltage change and supplies the needed current to the load. This lag in the time it takes for A to correct the load current and return the line to a quiescent high level is comprised of three elements: the natural response time of the A output, the delay associated with the trace length between the two outputs and the time it takes for a signal to propagate through the package. The trace delay can be effectively forced to zero by OR-tying adjacent pins. The resulting situation can then be considered "best case". In this best case situation if the delay through the package is not a significant portion of the transition time of the output the resulting negative going glitch will be relatively small (≈100mV). A disturbance of this size will not propagate through a system. As the trace length between OR-tied outputs increases, the magnitude of the negative going disturbance will increase. Older ECL families specified the maximum delay allowed between OR-tied outputs to prevent the creation of a glitch which would propagate through a system.

As this glitch phenomena is a physical limitation, due to decreased edge rates, ECLinPS devices are susceptible to the problem to an even greater degree than previous slower ECL families. The package delay of even the 28-lead PLCC

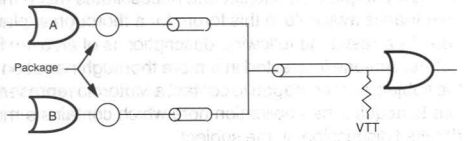


Figure 1.2 - Typical Wire-OR Configuration

is a significant portion of the transition times for an ECLinPS device. Therefore even in the best case situation described above one can expect an ≈200mV glitch on the OR-tied line. A glitch of this magnitude will not propagate through the system but it is significantly worse than the best case situation of earlier ECL families. In fact as long as the distance between OR-tied outputs is kept to less than 1/2" the resulting line disturbance will not be sufficient to propagate through most systems.

With this in mind the following recommendations are offered for OR-tying in ECLinPS designs. First OR-tying of clock lines should be avoided as even in the best case situation the disturbance on the line is significant and could cause false clocking in some situations. In addition wire-ORed outputs should be from the same package and preferably should be adjacent pins. Non adjacent outputs should be within 1/2" of each other with the load resistor connection situated near the midpoint of the trace (Figure 1.2). By following these guidelines the practice of wire-ORing ECL outputs can be expanded to the ECLinPS family without encountering problems in the system.

A detailed discussion of wire-OR connections in the ECLinPS world of performance is beyond the scope of this text. For this reason a separate application note has been written which deals with this situation in a much more thorough manner. Anyone planning to use wire-OR connections in their ECLinPS design is encouraged to contact a Motorola representative to obtain this application note.

Clock Distribution

Clock skew is a major contributor to the upper limit of operation of a high speed system, therefore any reduction in this parameter will enhance the overall performance of a system. Through the ECLinPS family and new offerings in the 10KH family Motorola is providing devices uniquely designed to meet the demands of low skew clock distribution.

By far the largest contributor to system skew is the variation between different process lots of a given device. This variation is what defines the total delay window specified in the data sheets. This window can be minimized if the devices are fully differential due to the output level defined thresholds which ensure a "centered" input swing. The propagation delay windows of single ended ECL and other logic technologies are intimately tied to variations in the input thresholds. As illustrated in Figure 1.3 although the delays when measured from the threshold of the input to the 50% point of the output are equal; when measured from the specified 50% point of the input to the 50% point of the output the delays will vary with any shift in the switching reference. Obviously the magnitude of the delay difference is also proportional to the edge rate of the input. In addition to increasing the size of the delay windows, this reference shift will cause the duty cycle of the output of a device to be different than that of the input. Unfortunately these thresholds are perhaps the most difficult aspects of a logic device to control. As a result for the ultimate in low skew performance differential ECL devices are a must. A quick perusal of the ECLinPS databook will reveal a relatively large number of totally differential devices which will lend themselves nicely to very low skew applications such as clock distribution.

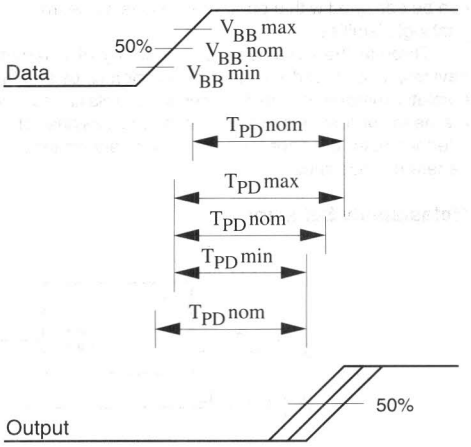


Figure 1.3 - Delay vs Switching Reference Offset

In addition to these generic differential devices there are several devices which were designed exclusively for clock distribution systems. With past ECL families designers were forced to build clock distribution trees with devices which were compromises at best. The ECLinPS family, however, was built around the E111 clock distribution chip; a fully differential 1:9 fanout device which boasts within part skews as well as part to part skews unequaled in today's market.

Additionally, to further deskew clock lines the E195 programmable delay chip is available. Although static delay lines can remove built in path length difference skew they can not compensate for variations in the delays of the devices in the clock path. The E195 allows the user to delay a signal over a 2ns range in ≈20ps steps. Through the use

of this device the designer can match skews between clocks to 20ps.

Although these two devices satisfy the needs for many ECL designers they do overlook the needs of a special subset; the designer who mixes ECL and TTL technologies. When translating between ECL and TTL much of the skew performance gained through the E111 is lost when passed through the translator and distributed in TTL. To solve this problem a new set of translators have been introduced in the MECL 10KH family. The H641 and H643 receive a differential ECL input and fan out nine TTL outputs with a guaranteed unparalleled skew between the TTL outputs. The H640 and H642 take differential ECL inputs and generate low skew TTL outputs which are ideal for driving clocks in 68030 and 68040 microprocessor systems. By using the ECL aspects of the E111 to distribute clock lines across the backplane to TTL cards and receiving and translating these signals with the H640, H641, H642 or H643 a TTL clock distribution tree can be designed with a performance level unheard of with past logic families.

Through the development of a library of differential devices, specialized low skew distribution chips and high resolution programmable delay chips Motorola has serviced the need for low skew clock distribution designs. These offerings open the door for even higher performance next generation machines.

Metastability Behavior

The metastability behavior and measurement of a flip flop is a complicated subject and necessitates much more time than is available in this forum for a thorough explanation. As a result the following description is of an overview nature. Anyone interested in a more thorough narration on the subject is encouraged to contact a Motorola representative to acquire the application note which contains a more detailed discussion on the subject.

In many designs occassions arise where an asynchronous signal needs to be synchronized to the system clock. Generally this task is accomplished with the use of a single or series of D flip flops as pictured in Figure 1.4. Because the data signal and the clock signal are asynchronous the system designer cannot guarantee that the setup and hold specifications for the device will be met. This in and of itself would not cause a problem if it was not for the metastable behavior of a D flip flop. The metastable behavior of a flip flop is described by the outputs of a device attaining a non-defined logic level or perhaps going into an oscillatory state when the data and the clock inputs to the flip flop switch simultaneously. It has been shown that this metastable behavior occurs across technology boundaries as well as across performance levels within a technology.

For ECL the characterisitic of a flip flop in a metastable state is a device whose outputs are in a non-defined state near the midpoint of a normal output swing. The output will return randomly to one of the two defined states some time later (Figure 1.5). The two parameters of importance when discussing metastability are the metastablity window; the

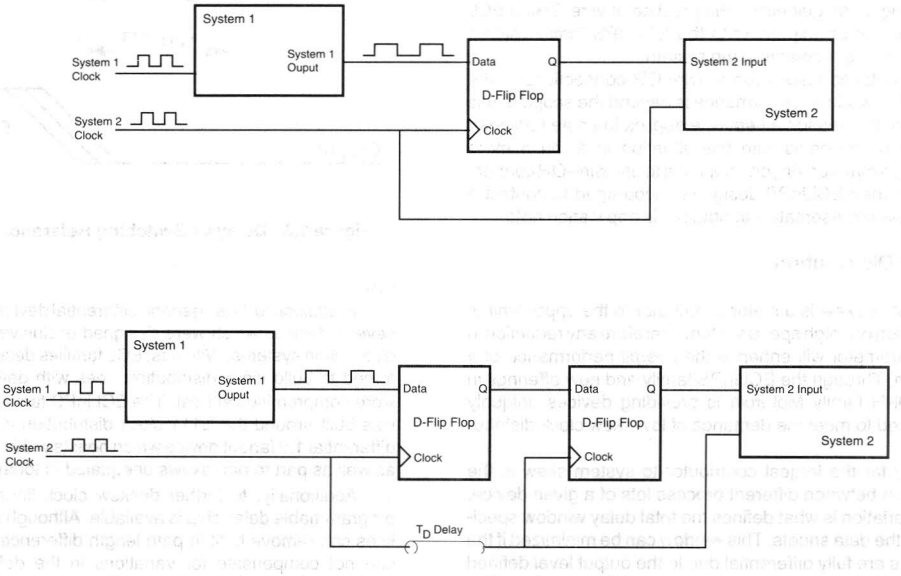


Figure 1.4 - Clock Synchronization Schemes

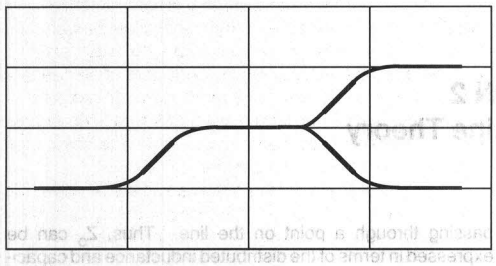


Figure 1.5 - Metastable Behavior of an ECL Flip Flop

window in time for which a transition on both the data and the clock will cause a metastable output, and the settling time; the time it takes for a metastable output to return to a defined state. For the single flip flop design of Figure 1.3, the data being fed into system 2 will be in an undefined state and thus unusable if the synchronizing flip flop enters a metastable state. Because of this a more popular design incorporates multiple flip flop chains with cascading data inputs and clock inputs which are delayed with respect to each other. This redundancy of flip flops helps to reduce the probability that the data entering system 2 will be at an undefined level which could wreak havoc on the logic of that system. This reduction in probability relies on the fact that even if the preceeding flip flop goes metastable it will settle to a defined state prior to the clocking of the following flip flop. Obviously once the first flip flop goes metastable there is an even chance that it will settle in the wrong state and thus information will be lost. However, there are error detection and correction methods to circumvent this problem. The larger the flip flop chain the lower the probability of metastable data being fed into system 2.

Unfortunately for ECLinPS levels of performance both the window width and the settling time are difficult or impossible to measure directly. The metastable window for an ECLinPS flip flop is assuredly less than 5ps and most likely less than 1ps based on SPICE level simulation results. In either case, with todays measuring equipment it would be impossible to measure this window width directly. Although it is feasible to measure the settling time for a given occurence, this parameter is not fixed but rather is of a variable length which makes it impossible to provide an absolute guarantee.

The challenge then becomes, how to characterize metastability behavior given the above circumstances. The standard method in the industry is to use Stoll's[1] equation, combined with the standard MTBF equation, to develop the following relationship:

$$MTBF = 1 / (2 * f_C * f_D * T_P * 10^{-(t/\tau)})$$

where:
- f_C: Clock Frequency
- f_D: Data Frequency
- T_P: FF Propagation Delay
- t: Time Delay Between FF Clocks
- τ: FF Resolution Time Constant

Note that the clock frequency, data frequency and time delay between flip flops are user defined parameters, thus it is up to Motorola to provide only the propagation delays and the resolution time constants for the ECLinPS flip flops.

The propagation delays are obviously already defined so this leaves only the resolution time constant yet to be determined. An evaluation fixture was fabricated and several ECLinPS flip flops were evaluated for resolution time constants. The results of the evaluation showed that the time constant was somewhat dependent on the part type as all the flip flops in the ECLinPS family do not use the same general design. The time constants range from 125 - 225 ps depending on the part type.

As an example for a system with a 100MHz clock and 75MHz data rate the required delay between clock edges of a cascaded flip flop chain for the E151 register, assuming a τ of 200ps, would be:

$$MTBF = 1 / (2 * 100MHz * 75MHz * 800ps * 10^{-t/200ps})$$

solving for an MTBF of 10 years yields:

$t = 3.1ns$ therefore:

$$T_D = \Delta t + T_P = 3.9ns$$

So for an MTBF of 10 years for the above situation the second flip flop should be clocked 3.9ns after the first. Similar results can be found by applying the equation to different data and clock rates as well as different acceptable MTBF rates.

[1]Stoll, P. "How to Avoid Synchronization Problems," VLSI Design, November/December 1982. pp. 56-59.

4

this picosecond region it becomes necessary to analyze system interconnects to determine if transmission line phenomena will occur. A handy rule of thumb to determine if an interconnect trace should be considered a transmission line is if the interconnect delay is greater than 1/8th of the signal transition time it should be considered a transmission line and afforded all of the attention required by a transmission line. If this rule is applied to the ECLinPS product line a typical PCB trace will attain transmission line behaviors for any length >1/4". Thus, a brief overview of transmission line theory is presented, including a discussion of distributed and lumped capacitance effects on transmission lines. For a more thorough discussion of transmission lines the reader is referred to Motorola's MECL Systems Design Handbook.

Background

Exact transmission line analysis can be both tedious and time consuming, therefore assumptions for simplifying these types of calculations must be made. A reasonable assumption is that interconnect losses caused by factors such as bandwidth limitations, attenuation, and distortion are negligible for a typical PCB trace. The basis for this assumption is that losses due to the interconnect conductor are only a fraction of the total losses in the entire interface scheme. In addition, the conductivity of insulating material is very small, as a result the dielectric losses are minimal. A second and more fundamental assumption is that transmission line behavior can be described by two parameters: line characteristic impedance (Z_O), and propagation delay (T_{PD}).

Characteristic Impedance

An interconnect which consists of two conductors and a dielectric, characterized by distributed series resistances and inductances along with distributed parallel capacitances between them, is defined as a transmission line. These transmission lines exhibit a characteristic impedance over any length for which the distributed parameters are constant. Since the contribution of the distributed series resistance to the overall impedance is minimal, this term can be neglected when expressing the characteristic impedance of a line. The characteristic impedance is a dynamic quantity defined as the ratio of the transient voltage to the transient current

$$Z_O = V/I = \sqrt{(L_O/C_O)} \quad \text{(eqt. 1)}$$

where:

L_O = Inductance per unit length (H)
C_O = Capacitance per unit length (F)

Propagation Delay

Propagation delay (T_{PD}) is also expressed as a function of both the inductance and capacitance per unit length of a transmission line. The propagation delay of the line is defined by the following equation:

$$T_{PD} = \sqrt{(L_O * C_O)} \quad \text{(eqt. 2)}$$

If L_O is expressed as microHenry's per unit length and capacitance as picoFarad's per unit length, the units for delay are nanoseconds per unit length. The propagation velocity is defined as the reciprocal of the propagation delay:

$$v = 1/T_{PD} = 1/\sqrt{(L_O * C_O)}$$

L_O and C_O can be determined using the easily measured parameters of line delay (T_D), line length (L), and the line characteristic impedance (Z_O) in conjunction with Equations 1 and 2. The propagation delay is defined as the ratio of line delay to line length:

$$T_{PD} = T_D/L$$

Combining equations 1 and 2 yields:

$$C_O = T_{PD}/Z_O \quad \text{(eqt. 3)}$$
$$L_O = T_{PD} * Z_O \quad \text{(eqt. 4)}$$

Termination and Reflection Theory

Figure 2.1 shows an ECLinPS gate driving a lossless transmission line of characteristic impedance Z_O, and terminated with resistance R_T. Modifying the circuit of Figure 2.1 such that the driving gate is represented by its equivalent circuit gives the configuration shown in Figure 2.2.

For a positive step function V_{IN}, a voltage step V_S travels down the transmission line. The initial current in the transmission line is determined by the ratio V_S/Z_O. When the

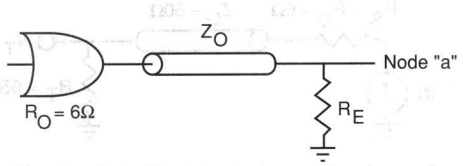


Figure 2.1 - Typical Transmission Line Driving Scenario

traveling wave arrives at the termination resistor R_T, Ohm's Law must be maintained. If the line characteristic impedance and the termination resistance match(i.e. Z_O=R_T), the traveling wave does not encounter a discontinuity at the line-load interface; thus the total voltage across the termination resistance is the incident voltage V_S. However, if mismatches between the line characteristic impedance and the termination resistance occur, a reflected wave must be set up to ensure Ohm's Law is obeyed at the line-load interface. In addition, the reflected wave may also encounter a discontinuity at the interface between the transmission line and the source resistance, thereby sending a re-reflected wave back towards the load. When neither the source nor the load impedance match the line characteristic impedance multiple reflections occur with the reflected signals being attenuated with each passage over the transmission line. The output response of this configuration appears as a damped oscillation, asymptotically approaching the steady state value, a phenomenon often referred to as ringing.

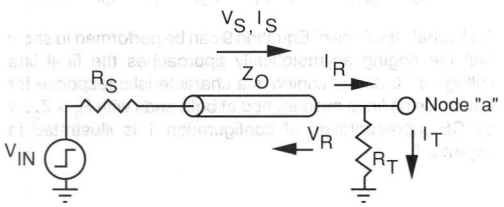


Figure 2.2 - Thevenin Equivalent Circuit of Figure 2.1

In performing transmission line analysis, designers may encounter one of three impedance situations:

1. $R_S < Z_O$; $R_T \neq Z_O$
2. $R_S \leq Z_O$; $R_T = Z_O$
3. $R_S = Z_O$; $R_T \neq Z_O$

where:
R_S = Source Resistance
R_T = Termination Resistance

Case 1: $R_S < Z_O$; $R_T \neq Z_O$

The initial current in the transmission line is determined by the ratio V_S/Z_O. However, the final steady state current is determined by the ratio V_S/R_T; assuming ohmic losses in the transmission line are negligible. For case 1, an impedance discontinuity exists at the line-load interface which causes a reflected voltage and current to be generated at the instant the initial signal arrives at this interface. To determine the fraction of the traveling wave that will be reflected from the line-load interface, Kirchoff's current law is applied to node "a" in Figure 2.2. This results in the following:

$I_T = I_S + I_R$ where:

$I_T = V_T/R_T$
$I_S = V_S/Z_O$
$I_R = -V_R/Z_O$

Using substitution:

$$V_T/R_T = V_S/Z_O - V_R/Z_O \qquad \text{(eqt. 5)}$$

Since only one voltage can exist at node "a" at any instant in time:

$$V_T = V_S + V_R \qquad \text{(eqt. 6)}$$

Combining Equations 5 and 6, and solving for V_R yields:

$$(V_S + V_R)/R_T = V_S/Z_O - V_R/Z_O$$

$$V_R = ((R_T - Z_O)/(R_T + Z_O))*V_S$$

$$V_R/V_S = \rho_L = (R_T - Z_O)/(R_T + Z_O) \qquad \text{(eqt. 7)}$$

Therefore:

$$V_R = \rho_L * V_S$$

The term ρ_L, referred to as the load reflection coefficient, represents the fraction of the voltage wave arriving at the line-load interface that is reflected back toward the source.

Similarly, a source reflection coefficient can be derived as:

$$\rho_S = (R_S - Z_O)/(R_S + Z_O) \qquad \text{(eqt. 8)}$$

From equations 7 and 8 it is apparent that multiple reflections will occur when neither the source nor the load impedances match the characteristic impedance of the line. A general equation for the total line voltage as a function of time and distance is expressed by Equation 9.

$$V(x,t) = V_A(t)*[U(t-T_{PD}*x) + \rho_L*U(t-T_{PD}(2L-x) + \rho_L*\rho_S*U(t-T_{PD}(2L+x)) + (\rho_L**2)*(\rho_S*U(t-T_{PD}(4L-x)) +$$

$(\rho_L{}^{**}2)*\rho_S{}^{**}2)*U(t-T_{PD}(4L+x)) + ...] + V_{DC}$ (eqt. 9)

where:
V_A = Voltage Entering the Transmission Line
T_{PD} = Propagation Delay of the Line
L = Total Line Length
x = Distance to an Arbitrary Point on the Line
V_{DC} = Initial Quiescent Voltage of the Line

Finally, the output voltage, V_T, can be derived from the reflection coefficient by combining Equations 6 and 7:

$$V_T=(1+(R_T-Z_O)/(R_T+Z_O))*V_S$$

$$V_T=(2*R_T/(R_T+Z_O))*V_S$$

The two possible configurations for the Case 1 conditions are $R_T>Z_O$ and $R_T<Z_O$. The following paragraphs will describe these two conditions in detail.

Configuration 1: $R_T > Z_O$

For the case in which $R_T>Z_O$, ρ_L is positive, and the initial current at node "a" is greater than the final quiescent current:

$$I_{INITIAL} > I_{FINAL}$$

Hence:

$$(V_S/Z_O)>(V_S/R_T)$$

Thus a reflected current, I_R, must flow toward the source in order to attain the final steady state current as shown in Figure 2.3.

An example of a line mismatched at both ends, with the

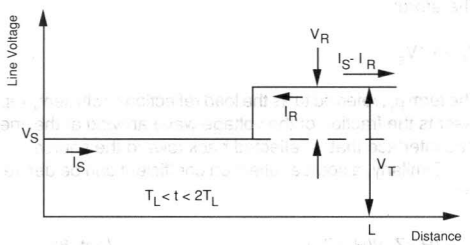


Figure 2.3 - Reflected Voltage Wave for $R_T > Z_O$

termination resistance greater than the load resistance is shown in Figure 2.4. The initial steady state output voltage is given by:

$$V_{TI} = (65/71)*(-1.75) = -1.60V$$

The final steady state output voltage is given by:

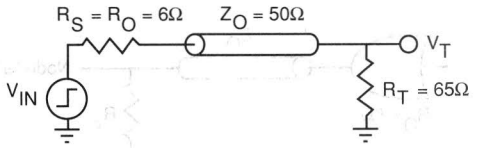


Figure 2.4 - Transmission Line Model for $R_T > Z_O$

$$V_{TF} = (65/71)*(-0.9) = -0.82V$$

The input voltage is a ramp from -1.75V to -0.9V. The initial voltage traveling down the line is:

$$V_S = (50/56)*0.85 = 0.76V$$

From Equations 7 and 8:

$$\rho_L = (R_T-Z_O)/(R_T+Z_O) = (65-50)/(65+50) = 0.13$$

$$\rho_S = (R_S-Z_O)/(R_S+Z_O) = (6-50)/(6+50) = -0.79$$

From Equation 9, the output voltage V_T after one line delay is:

$$V_T(L,T_{PD}) = V_A(t)*[1 + \rho_L] + V_{DC} = -0.71V$$

Likewise, after a time equal to three times the line delay, the output voltage V_T is

$$V_T(L,3T_{PD}) = V_A(t)*[\rho_L{}^*\rho_S + \rho_L{}^{**}2{}^*\rho_S] + V_T(L,T_{PD}) = -0.83V$$

Additional iterations of Equation 9 can be performed to show that the ringing asymptotically approaches the final line voltage of -0.82V. Ringing is a characteristic response for transmission lines mismatched at both ends with $R_T > Z_O$. A SPICE representation of configuration 1 is illustrated in Figure 2.5.

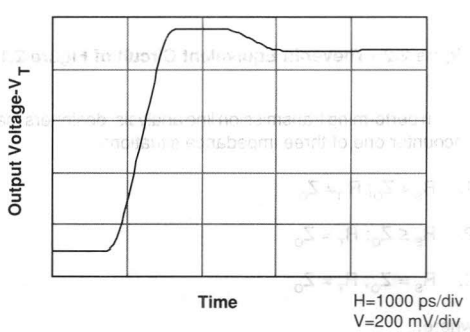


Figure 2.5 SPICE Results for Circuit of Figure 2.4

Configuration 2: $R_T < Z_O$

For the case in which $R_T<Z_O$, ρ_L is negative, and the initial current at node "a" is less than the final quiescent current.

$I_{INITIAL} < I_{FINAL}$

Hence:

$(V_S/Z_O) < (V_S/R_T)$

The reflected current, I_R, flows in the same direction as the initial source current in order to attain the final steady state current. The unique characteristic of configuration 2 is the negative reflection coefficient at both the source and load ends of the transmission line (Figure 2.6). Thus, signals approaching either end of the line are reflected with opposite polarity. In addition, the line voltage is a function of the pulse duration yielding steps of decreasing magnitude for input pulse durations greater than the line delay, and a series of attenuated pulses for input pulse durations less than the line delay.

An example of a line mismatched at both ends, with the

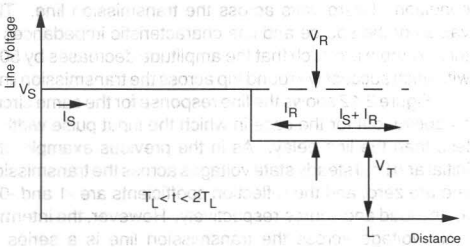


Figure 2.6 - Reflected Voltage Wave for $R_T < Z_o$

termination resistance less than the line resistance, and the input pulse width greater than the line delay is shown in Figure 2.7. The initial steady state output voltage is defined as:

$V_{TI} = (35/41)*(-1.75) = -1.49V$

The final steady state output voltage is given by

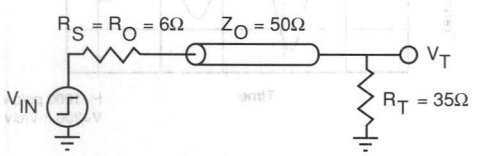


Figure 2.7 - Transmission Line Model for $R_T < Z_o$

$V_{TF} = (35/41)*(-0.9) = -0.77V$

For an input pulse from -1.75V to -0.9V the initial voltage traveling down the line is:

$V_S = (50/56)*0.85 = 0.76V$

From Equations 7 and 8,

$\rho_L = (35-50)/(35+50) = -0.18$

$\rho_S = (6-50)/(6+50) = -0.79$

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)*[1 + \rho_L] + V_{DC} = -0.87V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD}) = V_A(t)*[\rho_L*\rho_S + \rho_L**2*\rho_S] + V_T(L,T_{PD}) = -0.78V$

Additional iterations of Equation 9 can be performed to show that the output response asymptotically approaches -0.77 volts. Stair-steps are characteristic responses for transmission lines mismatched at both ends with $R_T < Z_O$, and a pulse width greater than the line delay. Figure 2.8 shows the results of a SPICE simulation for the case described by configuration 2.

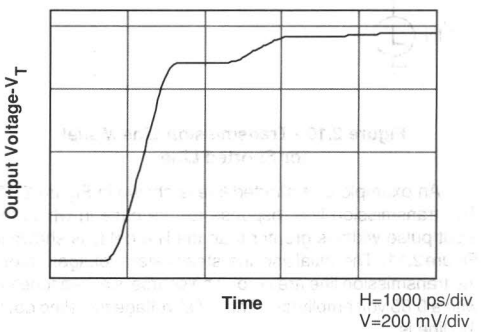


Figure 2.8 - SPICE Results for Circuit of Figure 2.7 with Input Pulse Width > Line Delay

Figure 2.9 shows the line response for the same circuit as above, but for the case in which the input pulse width is less than the line delay. As in the previous example, the initial steady state voltage across the transmission line is -1.49 volts, and the reflection coefficients are -0.18 and -0.79 for the load and source respectively. However, the intermediate

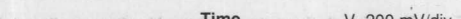


Figure 2.9 - SPICE Results for Circuit of Figure 2.7 with Input Pulse < Line Delay

voltage across the transmission line is a series of positive-going pulses of decreasing amplitude for each round trip of the reflected voltage, until the final steady state voltage of -1.49 volts is reached.

Shorted Line

The shorted line is a special case of configuration 2 in which the load reflection coefficient is -1, and the reflections tend toward the steady state condition of zero line voltage and a current defined by the source voltage and the source resistance.

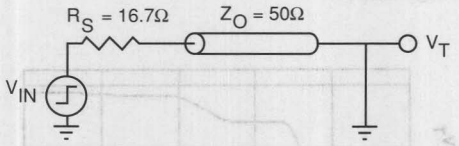


Figure 2.10 - Transmission Line Model for Shorted Line

An example of a shorted line is shown in Figure 2.10. The transmission line response for the case in which the input pulse width is greater than the line delay is shown in Figure 2.11. The initial and final steady state voltages across the transmission line are zero. The source is a step function with a 0.85 volt amplitude. The initial voltage traveling down the line is:

$V_s = (50/66.7)*0.85 = 0.64V$

From Equations 7 and 8,

$\rho_L = (0-50)/(0+50) = -1$

$\rho_s = (16.7-50)/(16.7+50) = -0.5$

Upon reaching the shorted end of the line, the initial voltage waveform is inverted and reflected toward the source. At the

Figure 2.11 - SPICE Results for Shorted Line with the Input Pulse Width > Line Delay

source end the voltage is partially reflected back toward the shorted end in accordance with the source reflection coefficient. Thus, the voltage at the shorted end of the transmission line is always zero while at the source end the voltage is reduced for each round trip of the reflected voltage. The voltage at the source end tends toward the final steady state condition of zero volts across the transmission line. The values of the source and line characteristic impedances in this example are such that the amplitude decreases by 50% with each successive round trip across the transmission line.

Figure 2.12 shows the line response for the same circuit as above, but for the case in which the input pulse width is less than the line delay. As in the previous example, the initial and final steady state voltages across the transmission line are zero, and the reflection coefficients are -1 and -0.5 for the load and source respectively. However, the intermediate voltage across the transmission line is a series of negative pulses with the amplitude of each pulse decreasing for each round trip of the reflected voltage until the final steady state voltage of zero volts is attained. Again, for this example the amplitude of the output response decreases by

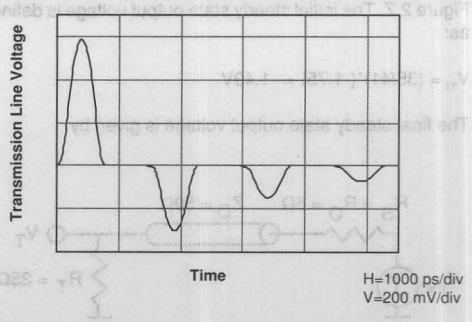


Figure 2.12 - SPICE Results for Shorted Line with the Input Pulse Width < Line Delay

50% for each successive reflection due to the choice of source and transmission line characteristic impedances.

Case 2: $R_S \leq Z_O$; $R_T = Z_O$

As in Case 1, the initial current in the transmission line is determined by the ratio of V_S/Z_O. Similarly, since $R_T = Z_O$ the final steady state current is also determined by the ratio V_S/Z_O. Because a discontinuity does not exist at the line-load interface all the energy in the traveling step is absorbed by the termination resistance, in accordance with Ohm's Law. Therefore no reflections occur and the output response is merely a delayed version of the input waveform.

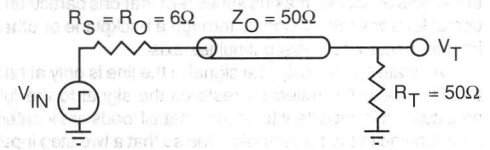


Figure 2.13 - Transmission Line Model for Matched Termination

An example of a line mismatched at the source but matched at the load is shown in Figure 2.13. For an input pulse of -1.75V to -0.9V is given by:

$V_{TI} = (50/56)*(-1.75) = -1.56V$

The final steady state output voltage is given by

$V_{TF} = (50/56)*(-0.9) = -0.80V$

The source is a step function with an 0.85 volt amplitude. The initial voltage traveling down the line is:

$V_S = (50/56)*0.85 = 0.76V$

From Equations 7 and 8,

$\rho_L = (50-50)/(65+50) = 0$

$\rho_S = (6-50)/(6+50) = -0.79$

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)*[1 + \rho_L] + V_{DC} = -0.80V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD}) = V_A(t)*[\rho_L*\rho_S + \rho_L**2*\rho_S] + V_T(L,T_{PD}) = -0.80V$

Thus the output response attains its final steady state value (Figure 2.14) after only one line delay when the termination

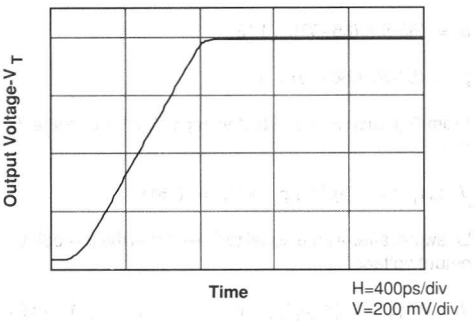


Figure 2.14 - SPICE Results for Matched Termination

resistance matches the line characteristic impedance. Ringing or stair-step output responses do not occur since the load reflection coefficient is zero.

Case 3: $R_s = Z_o$; $R_T \neq Z_o$

When the termination resistance does not match the line characteristic impedance reflections arising from the load will occur. Fortunately, in case 3, the source resistance and the line characteristic impedance are equal, thus the reflection coefficient is zero and the energy in these reflections is completely absorbed at the source thus no further reflections occur.

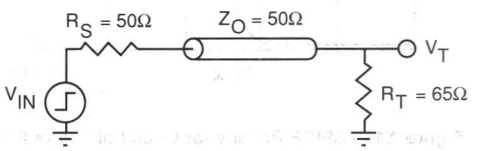


Figure 2.15 - Transmission Line Model for $V_s = Z_o$

An example of a line mismatched at the load but matched at the source is shown in Figure 2.15. For an input pulse of -1.75V to -0.9V the initial steady state output voltage is given by:

$V_{TI} = (65/115)*(-1.75) = -0.99V$

The final steady state output voltage is given by

$V_{TF} = (65/115)*(-0.9) = -0.51V$

The source is a step function with a 0.85 volt amplitude. The initial voltage traveling down the line is:

$V_S = (50/100)*0.85 = 0.43V$

From Equations 7 and 8,

ρ_L = (65-50)/(65+50) = 0.13

ρ_S = (50-50)/(50+50) = 0

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)*[1 + \rho_L] + V_{DC} = -0.51V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD}) = V_A(t)*[\rho_L*\rho_S + \rho_L**2*\rho_S] + V_T(L,T_{PD}) = -0.51V$

Thus the output response attains its final steady state value after one line delay when the source resistance matches the line characteristic impedance. Again, ringing or a stair-step output does not occur since the load reflection coefficient is zero (Figure 2.16).

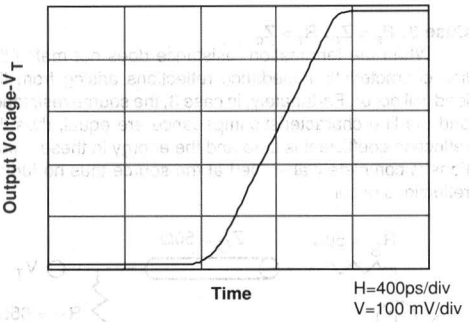


Figure 2.16 - SPICE Results for Circuit of Figure 2.15

Series Termination

Series termination represents a special subcategory of Case 3 in which the load reflection coefficient is +1 and the source resistance is made equal to the line characteristic impedance by inserting a resistor, R_{ST}, between and in series with, the transmission line and the source resistance R_O. The reflections tend toward the steady state conditions of zero current in the transmission line, and an output voltage equal to the input voltage. This type of termination is illustrated by the circuit configuration of Figure 2.17. The initial voltage down the line will be only half the amplitude of the input signal due to the voltage division of the equal source and line impedances.

$V_S = (Z_O/(2*Z_O))*V_{IN} = V_{IN}/2$ (eqt. 10)

The load reflection coefficient tends to unity, thus a voltage wave arriving at the load will double in amplitude, and a reflected wave with the same amplitude as the incident

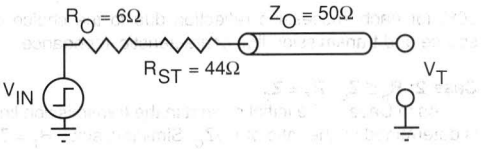


Figure 2.17 - Series Terminated Transmission Line

wave will be reflected toward the source. Since the source resistance matches the line characteristic impedance all the energy in the reflected wave is absorbed, and no further reflections occur. This "source absorption" feature reduces the effects of ringing, making series terminations particularly useful for transmitting signals through a backplane or other interconnects where discontinuities exist.

As stated previously, the signal in the line is only at half amplitude and the reflection restores the signal to the full amplitude. It is important to ensure that all loads are located near the end of the transmission line so that a two step input signal is not seen by any of the loads.

For the series terminated circuit of Figure 2.17 with $R_O + R_{ST} = Z_O$ and an input pulse rising from -1.75V to -0.9V, the initial line voltage V_{TI} is -1.325V and the final line voltage, V_{TF}, is -0.9V. The source is a step function with a 0.85 volt amplitude. The initial voltage traveling down the line is:

V_S = (50/100)*0.85 = 0.43V

From Equations 7 and 8,

ρ_L = (∞-50)/(∞+50) = 1

ρ_S = (50-50)/(50+50) = 0

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)*[1 + \rho_L] + V_{DC} = -0.9V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD}) = V_A(t)*\rho_L*\rho_S + \rho_L**2*\rho_S] + V_T(L,T_{PD}) = -0.9V$

Since the load reflection coefficient is unity, the voltage at the output attains the full ECL swing, whereas the voltage at the beginning of the transmission line does not attain this level until the reflected voltage arrives back at the source termination (Figures 2.17 and 2.18). No other reflections occur because the source impedance and line characteristic impedance match.

Capacitive Effects on Propagation Delay

Lumped Capacitive Loads

The effect of load capacitance on propagation delay

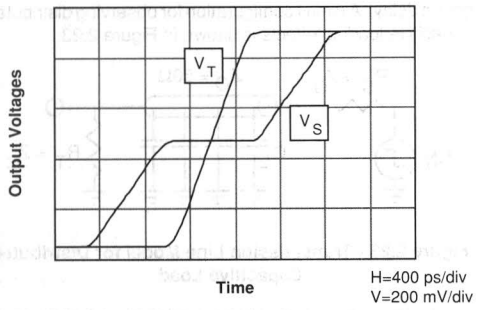


Figure 2.18 - SPICE Results for Series Terminated Line

must be considered when using high performance integrated circuits such as the ECLinPS family. Although capacitive loading affects both series and parallel termination schemes, it is more pronounced for the series terminated case. Figure 2.19a illustrates a series terminated line with a capacitive load C_L. Under the no load condition, C_L=0, the delay between the 50% point of the input waveform to the

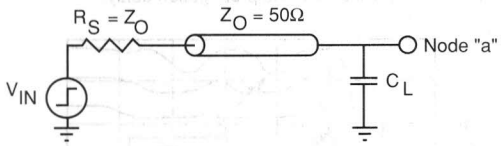


Figure 2.19a - Lumped Load Transmission Line Model

50% point of the output waveform is defined as the line delay T_D. A capacitive load placed at the end of the line increases the risetime of the output signal,thereby increasing T_D by an amount ΔT_D (Figure 2.19b). Figure 2.20 shows the increase

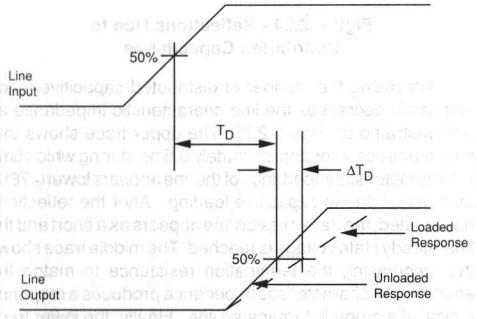


Figure 2.19b - ΔTD Introduced by Capacitive Load

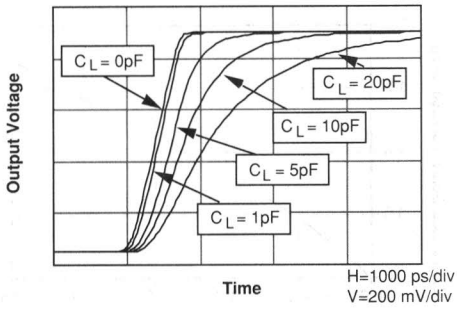


Figure 2.20 - Line Delay vs Lumped Capacitive Load

in delay for load capacitances of 0, 1, 5, 10 and 20 picoFarads.

The increase in propagation delay can be determined by using Thevenin's theorem to convert the transmission line into a single time constant network with a ramp input voltage. The analysis applies to both series and parallel terminations, since both configurations can be represented as a single time constant network with a time constant, τ, and a Thevenin impedance Z'.

Figure 2.21 shows the Thevenized versions for the series and parallel terminated configurations. The Thevenin impedance for the series configuration is approximately twice that for the parallel terminated case, thus the time constant will be two times greater for the series terminated configuration. Since τ is proportional to the risetime, the risetime will also be two times greater;thus the reason for the larger impact of capacitive loading on the series terminated configuration.

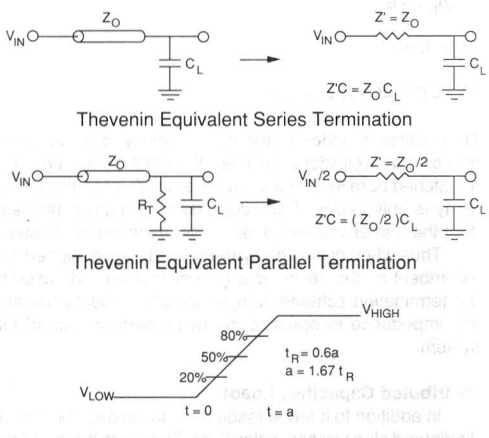


Figure 2.21 - Thevenin Equivalent Lumped Capacitance Circuits

0.0 0.5 1.0 1.5 2.0 2.5

Normalized Line-Load Time Constant ($Z'C / t_R$)

Figure 2.22 - Normalized Delay Increase Due to Lumped Capacitive Load

The relationship between the change in delay and the line-load time constant is shown in Figure 2.22. Both the delay change(ΔT_D) and the line-load time constant(Z'C) are normalized to the 20-80% risetime of the input signal. This chart provides a convenient graphical approach for approximating delay increases due to capacitive loads as illustrated by the following example.

Given a 100Ω series terminated line with a 5pF load at the end of the line and a no load rise time of 400ps the increase in delay, ΔT_D, can be determined using Figure 2.22. The normalized line-load time constant is:

$Z'C/t_R = 100\Omega * 5pF/400ps = 1.25$

Using this value and Figure 2.22:

$\Delta T_D/t_R = 0.9$

Therefore:

$\Delta T_D = 0.9 * 400ps = 360ps$

Thus 360ps is added to the no load delay to arrive at the approximate delay for a 5pF load. For a 100Ω line employing a matched parallel termination scheme, Z'=50Ω, the added delay is only 240ps. This added delay is significantly less than the one encountered for the series terminated case.

Thus when critical delay paths are being designed it is incumbent on the designer to give special consideration to the termination scheme, lumped loading capacitance and line impedance to optimize the delay performance of the system.

Distributed Capacitive Loads

In addition to lumped loading, capacitive loads may be distributed along transmission lines. There are three consequences of distributed capacitive loading of transmission lines: reflections, lower line impedance, and increased propagation delay. Each capacitive load connected along a transmission line causes a reflection of opposite polarity to the incident wave. If the loads are spaced such that the risetime is greater than the time necessary for the incident wave to travel from one load to the next, the reflected waves from two adjacent loads will overlap. Figure 2.24 shows the output response for a transmission line with two distributed capacitive loads of 2pF separated by a line propagation time of 750ps. The upper trace, with a 20-80% input signal risetime of 400ps, shows two distinct reflections. The middle and lower traces with 20-80% risetimes of 750 ps and 950ps respectively, show that overlap occurs as the risetime becomes longer than the line propagation delay.

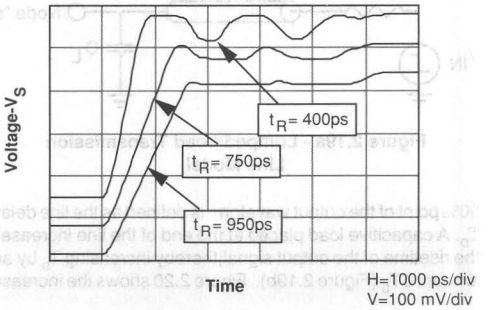


Figure 2.24 - Reflections Due to Distributed Capacitance

Increasing the number of distributed capacitive loads effectively decreases the line characteristic impedance as demonstrated by Figure 2.25. The upper trace shows that reflections occur for approximately 3.5 ns, during which time the characteristic impedance of the line appears lower(≈76Ω) than actual due to capacitive loading. After the reflections have ended, the transmission line appears as a short and the final steady state voltage is reached. The middle trace shows that decreasing the termination resistance to match the effective line characteristic impedance produces a response typical of a properly terminated line. Finally, the lower trace shows that the original steady state output can be attained by changing the source resistance to match the load resis-

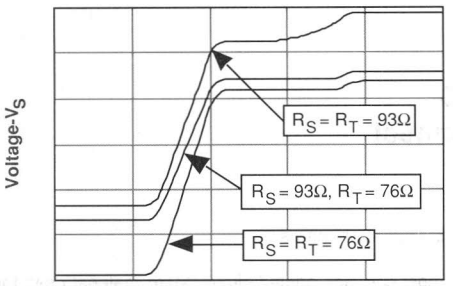


Figure 2.25 - Characteristic Impedance Changes Due to Distributed Capacitive Loads

tance and the effective characteristic capacitance.

Reduced Line Characteristic Impedance

To a first order approximation the load capacitance(C_L) is represented as an increase in the intrinsic line capacitance along that portion of the transmission line for which the load capacitances are distributed. If the length over which the load capacitances are distributed is defined as "L" the distributed value of the load capacitance(C_D) is given by

$$C_D = C_L/L \qquad \text{(eqt. 11)}$$

The reduced line impedance is obtained by adding C_D to C_O in Equation 1.

$$Z_O = \sqrt{(L_O/C_O)}$$

$$Z_O' = \sqrt{(L_O/(C_O + C_D))} = \sqrt{(L_O/(C_O*(1+C_D/C_O)))}$$

$$Z_O' = Z_O/\sqrt{(1 + C_D/C_O)} \qquad \text{(eqt. 12)}$$

For the circuit used to obtain the traces in Figure 2.25, the distributed load capacitance is 4pF. From Equation 3, C_O is calculated as

$$C_O = 750 \text{ ps}/93\Omega = 8\text{pF}$$

Hence:

$$Z_O' = 93\Omega/\sqrt{(1 + 4\text{pF}/8\text{pF})} = 76\Omega$$

Thus the effective line impedance is 17Ω lower than the actual impedance while reflections are occurring on the line.

Line Delay Increase

The increase in line delay caused by distributed loading is calculated by adding the distributed capacitance (C_D) to the intrinsic line capacitance in Equation 2.

$$T_{PD} = \sqrt{(L_O*C_O)}$$

$$T_{PD}' = \sqrt{(L_O*(C_O+C_D))}$$

$$T_{PD}' = T_{PD}*\sqrt{(1 + C_D/C_O)} \qquad \text{(eqt.13)}$$

Once again for the circuit used to obtain the traces in Figure 2.25, the distributed load capacitance is 4pF. From the previous example the intrinsic line capacitance is 8 pF therefore,

$$T_{PD}' = 750\text{ps}*\sqrt{(1 + 4\text{pF}/8\text{pF})} = 919\text{ps}$$

Thus, the effect of distributed load capacitance on line delay is to increase the delay by 169ps. From Equation 13 it is obvious that the larger the C_O of the line the smaller will be the increase in delay due to a distributive capacitive load. Therefore, to obtain the minimum impedance change and lowest propagation delay as a function of gate loading, the lowest characteristic impedance line should be used as this results in a line with the largest intrinsic line capacitance.

SECTION 3
System Interconnect

Introduction

As mentioned earlier, edge rates of the ECLinPS family are such that most interconnects must be treated as transmission lines. Thus, a controlled impedance environment is necessary to produce predictable interconnect delays as well as limiting the reflection phenomena of undershoot and overshoot. The three most common techniques for circuit and/or system interconnect at high data rates are microstrip, stripline and coaxial cable; both microstrip and stripline are printed circuit board methods whereas coaxial cable is most often used for interconnecting different parts of a system which are separated by relatively large distances. For slower speed applications (<300MHz) a twisted pair scheme also works well. The scope of this writing will not include the twisted pair technique, however a detailed discussion of this topic can be found in the MECL System Design Handbook. Finally, wirewrap boards are not recommended for the ECLinPS family because the fast edge speeds exceed the capabilities of normal wirewrapped connections. Mismatches at the connections cause reflections which distort the fast signal, significantly reducing the noise immunity of the system and perhaps causing erroneous operation.

Printed Circuit Boards

Printed circuits boards (PCB's) provide a reliable and economical means of interconnecting electrical signals between system components. Printed circuit boards consist of a dielectric substrate over which the conducting printed circuit material is placed. Three major categories of printed circuit boards exist:

1. Single-sided boards
2. Double-sided boards
3. Multilayer boards

The most common printed circuit board material used for digital designs is a glass- epoxy laminate. These boards use a fiberglass dielectric with copper foils bonded to both sides of the dielectric material by an epoxy resin. Other substrate materials include a fiberglass dielectric with a polyimide resin and fiberglass dielectric with a teflon resin. For multilayer boards the inner layers are separated by sheets of prepreg which acts as both a dielectric material and a bonding agent between layers.

The choice of substrate material depends on the function for which the board will be used, the environment in which the board is to operate, and costs. Table 3.1 lists several physical qualities which characterize several of the the available PCB types. Each available substrate material has its own properties which makes it ideally suited for particular applications.

Glass-Epoxy

Possesses good moisture absorption, chemical , and heat resistance properties as well as mechanical strength over standard humidity and temperature ranges.The most widely used versions are G10 and FR4, the fire resistant version of G10.

Glass-Polyimide

Good for elevated temperature operation because of its tight tolerance of the coefficient of thermal expansion. Very hard material, so it may damage drilling equipment when being drilled.

Glass-Teflon

Good for use when a low dielectric material is required. Very soft material, so it may be difficult to build features

Material	Dielectric Constant	Dissipation Factor	Thermal Coefficient of Expansion	Tensile Modulus
Glass-Epoxy	4.8 (1MHz)	0.022 (1MHz)	13 - 16 (10^{-6}/°C)	2.5
PTFE	2.1 (10GHz)	0.0004 (10GHz)	224 (10^{-6}/°C)	0.05
Glass-Polyimide	4.5 (1MHz)	0.10 (1MHz)	12 - 14 (10^{-6}/°C)	2.8

Table 3.1 - Characterisitics of Common PCB Materials

requiring precise geometries. Relatively expensive material.

Microstrip

A microstrip line is the easiest printed circuit interconnect to fabricate because it consists simply of a ground plane and flat signal conductor separated by a dielectric (Figure 3.1).

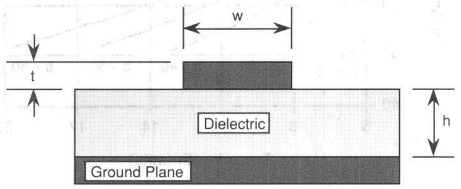


Figure 3.1 - Microstrip Line

The characteristic impedance, Z_O, of a microstrip line is given by:

$$Z_O = \frac{87}{\sqrt{(\varepsilon_r + 1.41)}} \ln\left[\frac{(5.98 * h)}{(0.8w + t)}\right] \qquad \text{(eqt. 1)}$$

where:

ε_r = Relative Dielectric Constant of the Substrate
w = Width of the Signal Trace
t = Thickness of Signal Trace
h = Thickness of the Dielectric

Equation 1 is accurate to within ±5% when:

$$0.1 < w/h < 3.0 \text{ and } 1 < \varepsilon_r < 15$$

To mitigate the effects of electric field fringing, an additional constraint is that the width of the ground plane be such that it extends past each edge of the signal line by at least the width of the signal line.

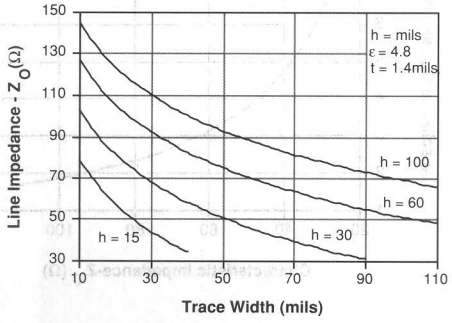
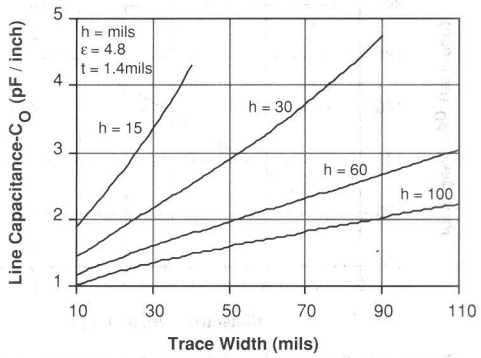


Figure 3.2 - Microstrip Impedance vs Trace Width



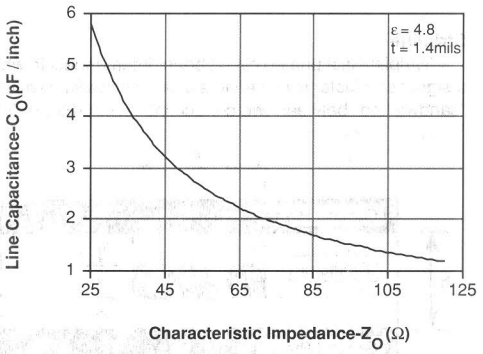


Figure 3.3 - Line Capacitance vs Line Impedance and Trace Width

Figure 3.2 is a plot of characteristic impedance as a function of trace width and dielectric thickness for a dielectric constant of 4.8 and a trace thickness of 1.4mils (1 ounce copper). Using the equation for C_O developed in the previous chapter and Equation 1 above the capacitance per unit length can be calculated for various trace widths. Figure 3.3 plots C_O vs trace width for several different dielectric thicknesses. In addition Figure 3.3 plots C_O vs the characteristic impedance for a microstrip line for the dielectric constant and trace thickness given above.

The propagation delay for a signal on a microstrip line is described by the following equation:

$$T_{PD} = 1.016\sqrt{(0.475 * \varepsilon_r + 0.67)} \quad \text{ns/foot} \qquad \text{(eqt 2)}$$

where:

ε_r = Dielectric Constant of the Board Material

Note that the propagation delay is dependent only on the dielectric constant of the PCB substrate. Figure 3.4 plots the propagation delay of a microstrip line versus the dielectric constant of the PCB.

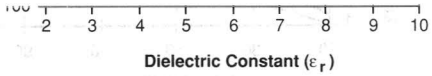


Figure 3.4 - Propagation Delay vs Dielectric Constant

Stripline

Stripline is a printed circuit board interconnect in which a signal conductor is placed in a dielectric medium which is "sandwiched" between two conducting layers (Figure 3.5).

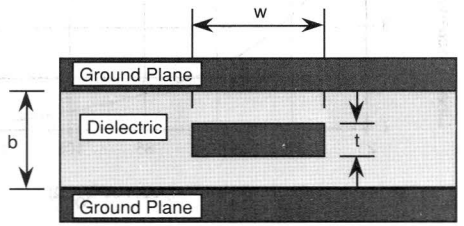


Figure 3.5 - Stripline Structure

The characteristic impedance of the stripline is given by:

$$Z_O = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4b}{0.67\pi(0.8w + t)}\right] \qquad \text{(eqt. 3)}$$

where:

ε_r = Relative Dielectric Constant of the Substrate
w = Width of the Stripline
t = Thickness of the Stripline
b = Distance Between the Two Ground Planes

Equation 3 is accurate for the following dimension ratios:

$w/(b - t) < 0.35$ and $t/b < 0.25$

Once again, using a fairly typical ε_r of 4.8 and a copper trace thickness of 1.4 mils, the characteristic impedance of a stripline interconnect can be plotted for various trace widths and dielectric thicknesses (Figure 3.6).

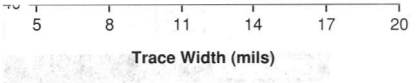


Figure 3.6 - Stripline Impedance vs Trace Width

As was the case with a microstrip line the capacitance per unit length of a stripline trace can be calculated using the C_O equation from Chapter 2. The graphs of Figure 3.7 plot

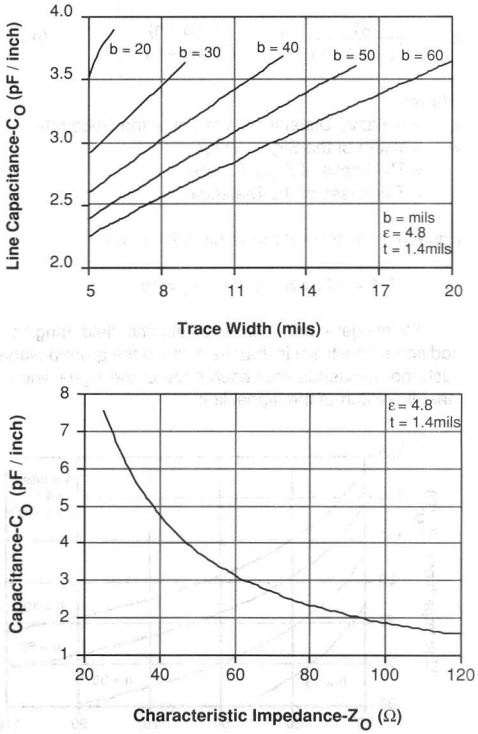


Figure 3.7 - Stripline Capacitance vs Impedance and Trace Width

the capacitance of a stripline structure for a number of trace widths as well as the C_O versus the characteristic impedance of the line.

The propagation delay of a stripline trace is governed by the simple equation:

$$T_{PD} = 1.016\sqrt{\varepsilon_r} \text{ ns/ft} \qquad \text{(eqt. 4)}$$

where:

ε_r = Dielectric Constant of the Board Material

Again the propagation delay of the trace is dependent only on the relative dielectric constant of the PCB substrate. Using Equation 4 the delay of the line can be plotted vs dielectric constant (Figure 3.8).

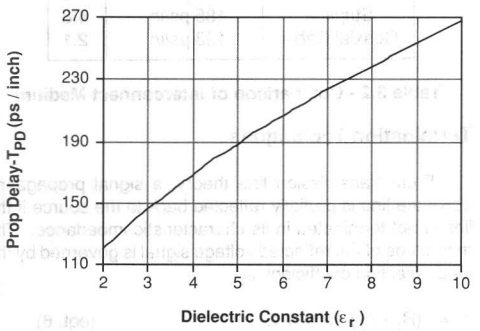


Figure 3.8 - Stripline Propagation Delay vs Dielectric Constant

General Information

Since fiberglass-epoxy is by far the most widely used substrate in the industry two important considerations should be mentioned:

1. The propagation delay for microstrip is ≈145 ps per inch whereas that for stripline is ≈185 ps per inch. Since the propagation delay is governed by the dielectric of the substrate, a board material with a lower dielectric constant than glass-epoxy is required if a lower propagation delay is desired.

2. Cross coupled noise due to board geometries may require a substrate material with a lower dielectric constant. For example, the distance from the signal trace to the ground plane is a function of the substrate dielectric constant for a specified line characteristic impedance. Hence the switching energy coupled into adjacent traces on the same signal plane is also a function of the dielectric constant. If the dielectric thickness and trace width must be maintained for a given line impedance, the spacing between traces must be increased to maintain the noise margin. Since the dielectric constant of glass-epoxy is relatively large, the increase in spacing between the traces may be unacceptable. So, a substrate material with a lower dielectric constant may be desirable. Generally if the distance between traces is maintained at twice the distance to the ground plane, coupling between traces will be minimal.

Finally, printed circuit signal line shape variations play a significant role in modulating both the capacitance and inductance per unit length for a transmission line; in other words shape variations cause reflections. Bends in printed circuit traces cause an increase in the capacitance per unit length and a decrease in the inductance per unit length with a pronounced effect for angles of 90° or more. Two techniques available to compensate for shape changes are:

1. Maintain a uniform trace width.

2. Cut the corners of the trace such that the length of the diagonal cut is in the range of 1.6 to 2.0 times the trace width.

Figure 3.9 illustrates these two techniques.

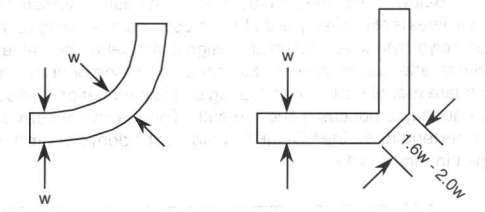


Figure 3.9 - Compensation for Capacitive Effects of Trace Angles

Coaxial Cable

Coaxial cable is a two conductor transmission line consisting of a concentric inner conductor surrounded by a dielectric which in turn is surrounded by a tubular outer conductor (Figure 3.10). It is ideal for transmitting high frequency signals over long distances because of its well defined and uniform characteristic impedance. Moreover, crosstalk is minimized by the ground shield provided by the outer conductor.

The propagation delay is derived in the same way as a stripline interconnect and thus is described by Equation 4. Therefore as with stripline structures the delay is a function

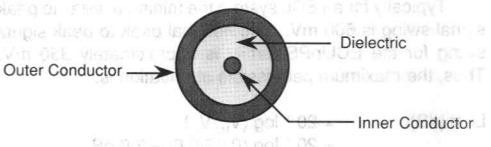


Figure 3.10 - Cross Section of Coaxial Cable

of only the dielectric constant. The characteristic impedance and capacitance per unit length are parameters specified by the coaxial cable manufacturer, hence the designer should look to the cable manufacturer for these parameters.

Coaxial Cable Lengths

The ECLinPS family operates with rise times as fast as several hundred picoseconds, thus coaxial cable must be able to transmit these pulses without introducing a significant distortion. Viewing the ECLinPS output as a single time constant driver circuit terminated with a 50Ω load, the required line bandwidth(f_C) can be calculated as follows.

$$f_C = 0.35/t_R \qquad \text{(eqt. 5)}$$

where:

t_R =10% to 90% Rise Time

Converting the typical 20%-80% rise time value of 400 ps to an equivalent 10%-90% rise time value of 530ps, and using Equation 5 yields a bandwidth value of f_C = 660MHz

Below 1 GHz the primary loss mechanism in transmission lines is skin effect, as dielectric losses for materials such as polyethylene and teflon are insignificant below this value. Since attenuation due to skin effect is proportional to the square root of frequency a log-log plot of attenuation versus frequency produces a linear result. The maximum coaxial cable lengths for the ECLinPS family can be derived from the plot in Figure 3.11.

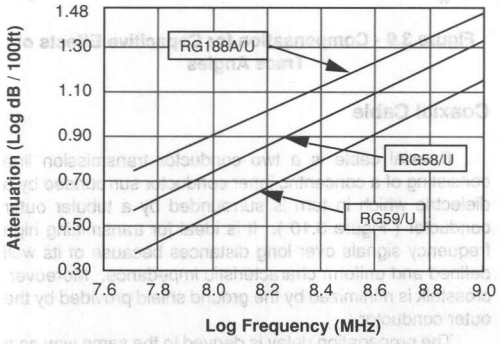


Figure 3.11 - Coaxial Cable Attenuation vs Frequency

Typically for an ECL system the minimum peak to peak signal swing is 600 mV. The nominal peak to peak signal swing for the ECLinPS family is approximately 850 mV. Thus, the maximum permissible attenuation is:

$$\text{Loss(dB)} = 20 * \log (V_{IN}/V_O)$$
$$= 20 * \log (0.85/0.6) = 3.0 \text{ dB}.$$

From Figure 3.11 the loss at 660MHz for RG58/U cable is 15 dB/ 100 feet. Therefore, the maximum length is

Max Length = 100 ft. * (3.0 dB/15 dB) = 20 ft.

Additional information concerning coaxial cable can be found in Motorola's MECL System Design Handbook.

Summary of Values

Table 3.2 is a compilation of propagation delays at nominal dielectric values for the three types of interconnects discussed.

Interconnect	T_{PD}	ε_r
Microstrip	145 ps/in	4.8
Stripline	185 ps/in	4.8
Coaxial Cable	123 ps/in	2.1

Table 3.2 - Comparison of Interconnect Medium

Termination Techniques

From transmission line theory, a signal propagating down the line is partially reflected back to the source if the line is not terminated in its characteristic impedance. The magnitude of the reflected voltage signal is governed by the load reflection coefficient, ρ_L.

$$\rho_L = (R_T - Z_O) / (R_T + Z_O) \qquad \text{(eqt. 6)}$$

where:

R_T = Load Impedance, and

Z_O = Characteristic Impedance of the Line

When the reflected signal arrives at the source it is re-reflected back toward the load with a magnitude dictated by the source reflection coefficient, ρ_S.

$$\rho_S = (R_S - Z_O) / (R_S + Z_O) \qquad \text{(eqt. 7)}$$

where:

R_S = Source Impedance

Z_O = Characteristic Impedance of the Line

The reflected signal continues to be re-reflected by the source and load impedances and is attenuated with each passage over the transmission line. The output response appears as a damped oscillation asymptotically approaching the steady state value. This phenomena is often referred to as ringing.

The importance of minimizing the reflected signals lies in their adverse affect on noise margin and the potential for driving the input transistors of the succeeding stage into saturation. Both of these phenomena can lead to less than ideal system performance. To minimize the potential hazards associated with reflections on transmission lines three

basic termination techniques are available:

1. Minimizing Unterminated line lengths
2. Parallel Termination
3. Series Termination

Unterminated Lines

Figure 3.12 illustrates an unterminated transmission line. This configuration is also referred to as a stub or an open line.

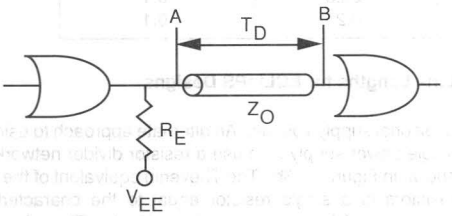


Figure 3.12 - Unterminated Transmission Line

The function of R_E is to provide the drive current for a high to low transition at the driver output. Since the reflection coefficient at the load is of opposite polarity to that at the source, the signal will be reflected back and forth over the transmission line with the polarity changing after each reflection from the source impedance. Thus, steps appear at the input tothe receiving gate. When R_E is too large steps appear in the trailing edge of the propagating signal that slows the edge speed of the input to the receiving gate, subsequently causing an increase in the net propagation delay. A reasonable negative-going signal swing at the input of the receiving gate results when the value of R_E is selected to produce an initial step of 600mV at the driving gate. Hence:

$$I * Z_O > 0.6 \qquad \text{(eqt. 8)}$$

$$(V_{OH} - V_{EE})/(R_E + Z_O) * Z_O \geq 0.6$$

$$6.2Z_O \geq R_E \ (10E)\ ,\ 4.9Z_O \geq R_E \ (100E) \qquad \text{(eqt. 9)}$$

Load resistors of less than 180Ω should not be used because the heavy load may cause a reduction in noise immunity when the output is in the high state due to an increased output emitter-follower V_{BE} drop.

When the driver gate delivers a full ECL swing, the signal propagates from point A arriving at point B a time T_D later. At point B the signal is reflected as a function of ρ_L. The input impedance of the receiving gate is large relative to the line characteristic impedance, therefore:

$$\rho_L = (R_T - Z_O) / (R_T + Z_O) \approx 1 \qquad \text{(eqt. 10)}$$

A large positive reflection occurs resulting in overshoot. The reflected signal reaches point A at time $2T_D$, and a large negative reflection results because the output impedance of the driver gate is much less than the line characteristic impedance (i.e. $R_O << Z_O$). In this case the reflection coefficient is negative.

$$\rho_S = (R_O - Z_O) / (R_O + Z_O) \qquad \text{(eqt. 11)}$$

The signal is re-reflected back toward the load arriving at time $3T_D$ resulting in undershoot at point B. This re-reflection of signals continues between the source and load impedances causing ringing to appear on the output response.

The impetus in restricting interconnect lengths is to mitigate the effects of overshoot and undershoot. A handy rule of thumb is that the undershoot can be limited to less than 15% of the logic swing if the two way line delay is less than the rise time of the pulse. With an undershoot of <15% the physics of the situation will result in an overshoot which will not cause saturation problems at the receiving input. Thus, the maximum line length can be determined using Equation 12.

$$L_{max} < t_R/2*T_{PD} \ \text{(unit length)} \qquad \text{(eqt. 12)}$$

where:
L = Line Length
t_R = Rise time
T_{PD}= Propagation Delay per unit Length

Further, the propagation delay increases with gate loading, thus the actual delay per unit length (T_{PD}') is given as:

$$T_{PD}' = T_{PD} * \sqrt{(1 + C_D / (L * C_O))}$$

Substitution of the modified delay per unit length into Equation 12 and rearranging yields Equation 13:

$$t_R \geq (2 * L) * T_{PD} * \sqrt{(1 + C_D / (L * C_O))} \qquad \text{(eqt. 13)}$$

Solving Equation 13 for the maximum line length produces:

$$L_{max} = 0.5 *(\sqrt{((C_D / C_O) ** 2 + (t_R/ T_{PD}) ** 2) - C_D/ C_O} \qquad \text{(eqt. 14)}$$

Assuming a worst case capacitance of 2 pF and a rise time of 200 ps for the ECLinPS family gives a value of 0.3 inches for the maximum open line length.

Table 3.3 shows maximum open line lengths derived from SPICE simulations for single and double gate loads, a maximum overshoot of 40% and undershoot of 20% was assumed. The simulation results indicate that for a 50Ω line a stub length of ≤ 0.3 inches will limit the overshoot to less than 40%, and the undershoot to within 20% of the logic swing. Signal traces will most assuredly be larger than .3" for all but the simplest of interconnects, thus for most practical applications it will be necessary to use ECLinPS devices in a controlled impedance environment.

Parallel Termination

When the fastest circuit performance or the ability to drive distributed loads is desired, parallel termination is the method of choice. An important feature of the parallel termination scheme is the undistorted waveform along the full length of the line. A parallel terminated line is one in which the receiving end is terminated to a voltage (V_{TT}) through a resistor (R_T) with a value equal to the line characteristic impedance (Figure 3.13a). An advantage of this technique is that power consumption can be decreased by a judicious choice of V_{TT}. For 50Ω systems the typical value of V_{TT} is negative two volts.

Although the single resistor termination to V_{TT} conserves power, it offers the disadvantage of requiring an additional supply voltage. An alternate approach to using a single power supply is to use a resistor divider network as shown in Figure 3.13b. The Thevenin equivalent of the two resistors is a single resistor equal to the characteristic impedance of the line, and terminated to V_{TT}. The values for resistors R_1 and R_2 may be obtained from the following relationships:

$$R_2 = (V_{EE} / V_{TT}) * Z_O \quad \text{(eqt. 15)}$$
$$R_1 = (R_2 * V_{TT})/(V_{EE}-V_{TT}) \quad \text{(eqt. 16)}$$

For a nominal 10E supply voltage of -5.2V and V_{TT} of -2V:

$$R_2 = 2.6 * Z_O \quad \text{(eqt. 17)}$$
$$R_1 = R_2 / 1.6 \quad \text{(eqt. 18)}$$

For a nominal 100E supply voltage of -4.5V and V_{TT} of -2V

$$R_2 = 2.25 * Z_O \quad \text{(eqt. 19)}$$
$$R_1 = R_2 / 1.25 \quad \text{(eqt. 20)}$$

Table 3.4 provides a reference of values for the resistor divider network of Figure 3.13b.

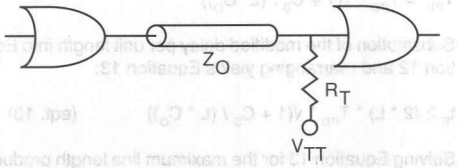


Figure 3.13a Parallel Termination to VTT

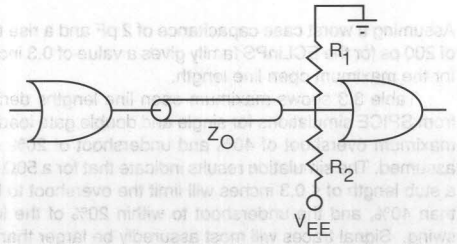


Figure 3.13b Thevenin Equivalent Parallel Termination

Figure 3.13 - Parallel Termination Schemes

ZO (Ω)	10E		100E	
	R_1 (Ω)	R_2 (Ω)	R_1 (Ω)	R_2 (Ω)
50	81	130	90	113
70	113	182	126	158
75	121	195	135	169
80	130	208	144	180
90	146	234	161	202
100	162	260	180	225
120	194	312	216	270
150	243	390	270	338

Table 3.4 - Thevenin Termination Resistor Values

levels are -0.930 volts at 20.0mA for the high state and -1.705volts at 5.9mA for the low state.

Figure 3.14 shows the nominal output characteristics for ECLinPS devices driving various load impedances returned to a negative two volt supply. This plot applies to both 10E and 100E versions of the ECLinPS family. The output resistances R_H (high state output resistance) and R_L (low state output resistance) are obtained from the reciprocal of the slope at the desired operating point. Many applications require loads other than 50Ω, the resulting V_{OH} and V_{OL} levels can be estimated using the following technique.

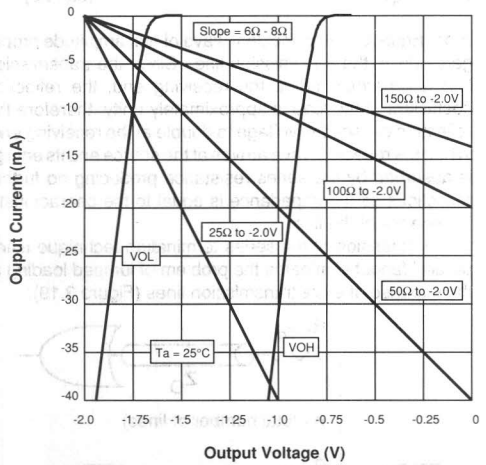


Figure 3.14 - ECLinPS Output Charactersitics

10E Devices

The equivalent output circuit is shown in Figure 3.15. The output levels are estimated from Figure 3.15 as follows:

$$V_{OH} = -770mV - 6*I_{HOUT} \quad \text{(eqt. 21)}$$

Figure 3.15 - Equivalent Model for Calculating 10E Output Levels

where:

$I_{HOUT} = (-770mV - V_{TT})/(6\Omega + R_T)$

and

$V_{OL} = -1710mV - 8*I_{LOUT}$ (eqt. 22)

where:

$I_{LOUT} = (-1710mV - V_{TT}) / (8\Omega + R_T)$

100E Devices

The equivalent output circuit is shown in Figure 3.16. The output levels are estimated from Figure 3.16 as follows:

$$V_{OH} = -830mV - 6*I_{HOUT} \quad \text{(eqt. 23)}$$

where:

$I_{HOUT} = (-830mV - V_{TT}) / (6\Omega + R_T)$

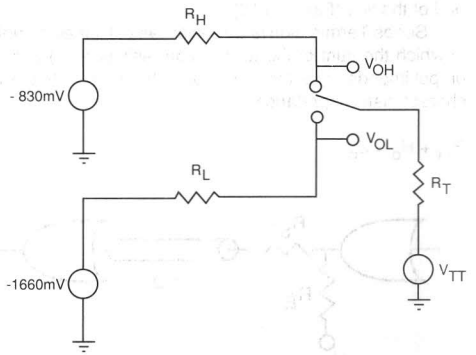


Figure 3.16 - Equivalent Circuit for Calculating 100E Output Levels

and

$V_{OL} = -1660mV - 8*I_{LOUT}$ (eqt. 24)

where:

$I_{LOUT} = (-1660mV - V_{TT})/(8\Omega + R_T)$

SIP Resistors

The choice of resistor type for use as the termination resistor has several alternatives. Although the use of a discrete, preferably chip resistor, offers the best isolation and lowest parasitic additions there are SIP resistor packs which will work fine for ECLinPS designs. SIP resistors offer a level of density which is impossible to obtain using their discrete counterparts. However, there are some guidelines which the user should follow when using SIP resistor packs. Always terminate complimentary outputs in the same pack to minimize inductance effects on the SIP power pin. Noise generated on this pin will couple directly into all of the resistors in the pack. In addition, the SIP package should incorporate bypass capacitors in the design (Figure 3.17). These capacitors are necessary to help maintain a solid V_{TT} level within the package, again mitigating any potential crosstalk or feedthrough effects. A 10 pin SIP like the DALE CSRC-10B21-500J/103M, is suitable for providing 50Ω terminations while maintaining a relatively noise free environment to non-switching inputs.

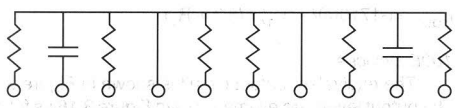


Figure 3.17 - Standard ECL 10 pin SIP

Series Termination Technique

Series Damping is a technique in which a termination resistance is placed between the driver and the transmission line with no termination resistance placed at the receiving end of the line (Figure 3.18).

Series Termination is a special case of series damping in which the sum of the termination resistor (R_{ST}) and the output impedance of the driving gate (R_O) is equal to the line characteristic impedance.

$R_{ST} + R_O = Z_O$

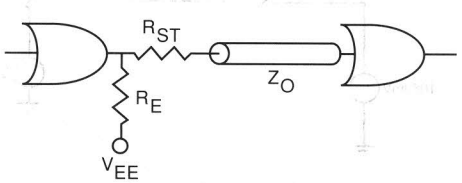


Figure 3.18 - Series Termination

As mentioned in the Transmission line section, series termination techniques are useful when the interconnect lengths are long or impedance discontinuities exist on the line. Additionally, the signal travels down the line at half amplitude minimizing problems associated with crosstalk. Unfortunately, a drawback with this technique is the possibility of a two step signal appearing when the driven inputs are far from the end of the transmission line. To avoid this problem the distance between the end of the transmission line and input gates should adhere to the guidelines specified in Table 3.3 from the section on unterminated lines.

Series Termination Theory

When the output of the series terminated driver gate switches, a change in voltage(ΔV_B) occurs at the input to the transmission line:

$\Delta V_B = V_{IN} * (Z_O) / (R_{ST} + R_S + Z_O)$ (eqt. 25)

where:

V_{IN} = Internal Voltage Change
Z_O = Line Characteristic Impedance
R_S = Output Impedance of the Driver Gate
R_{ST} = Termination Resistance

Since $Z_O = R_{ST} + R_S$ substitution into Equation 25 yields:

$\Delta V_B = V_{IN} / 2$ (eqt. 26)

From Equation 26 an incident wave of half amplitude propagates down the transmission line. Since the transmission line is unterminated at the receiving end, the reflection coefficient at the load is approximately unity; therefore the reflection causes the voltage to double at the receiving end. When the reflected wave arrives at the source end its energy is absorbed by the series resistance producing no further reflections as the impedance is equal to the characteristic impedance of the line.

A extension of the series termination technique using parallel fanout eliminates the problem of lumped loading at the expense of extra transmission lines (Figure 3.19).

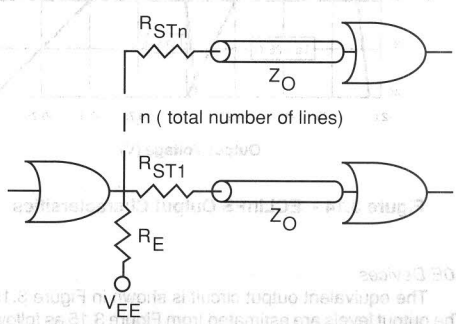


Figure 3.19 - Parallel Fanout using Series Termination

Calculation of R_E

R_E functions to establish V_{OH} and V_{OL} levels and to provide the negative going drive into R_{ST} and Z_O when the driver output switches to the low state. The value of R_E must be such that the required current is supplied to each transmission line while not allowing the output transistor to turn off when switching from a high to a low state. An appropriate model is to treat the output emitter follower as a simple switch (Figure 3.20).

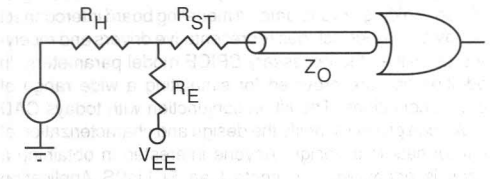


Figure 3.20 - Equivalent Circuit for R_E Determination

The worst case scenario occurs when the driver output emitter follower is cutoff during a negative going transition. When this happens the switch can be considered opened, and at the instant it opens the line characteristic impedance behaves as a linear resistor returned to V_{OH}. The model becomes a simple series resistive network as shown in Figure 3.21.

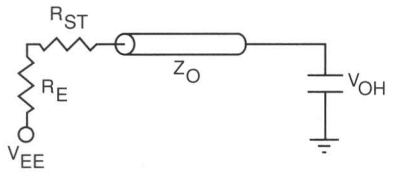


Figure 3.21 - Equivalent Circuit with Output Cutoff

The maximum current occurs at the instant the switch opens and is given by Equation 27.

$$I_{MAX} = (V_{OH} - V_{EE}) / (R_E + R_{ST} + Z_O) \qquad \text{(eqt. 27)}$$

The initial current must be sufficient to generate a transient voltage equal to half of the logic swing since the voltage at the receiving end of the line doubles for the series terminated case. To insure the pull down current is large enough to handle reflections caused by discontinuities and load capacitances the transient voltage is increased by 25%. Therefore,

$$I_{INIT} = (1.25 * V_{SWING}/2) / Z_O \qquad \text{(eqt. 28)}$$

To satisfy the initial constraints $I_{MAX} > I_{INIT}$

$$(V_{OH} - V_{EE}) / (R_E + R_{ST} + Z_O) > (1.25 * V_{SWING}/2) / Z_O$$

For the 10E series

V_{OH} = -0.9V, V_{SWING} = 0.85V, V_{EE} = -5.2V

$$[-0.9 - (-5.2)] / (R_{ST} + R_E + Z_O) \geq 0.531 / Z_O$$

$$7.10 * Z_O - R_{ST} \geq R_E \qquad \text{(eqt. 29)}$$

For the 100E series:

V_{OH} = -0.955V, V_{SWING} = 0.75, V_{EE} = -4.5V

$$6.56 * Z_O - R_{ST} > R_E \qquad \text{(eqt. 30)}$$

Figure 3.19 showed a modification of the series termination scheme in which several series terminated lines are driven by a single ECL gate. The principle concern when applying this technique is to maintain the current in the output emitter follower below the maximum rated value. The value for R_E can be calculated by viewing the circuit in terms of conductances.

$$G_E > G_1 + G_2 + ... + G_n \qquad \text{(eqt. 31)}$$

For the 10E series

$$1 / R_E \geq 1 / (7.10*Z_{O1} - R_{ST1}) + 1 / (7.10*Z_{O2} - R_{ST2}) + 1 / (7.10*Z_{O3} - R_{STn})$$

For the case where $Z_{O1}=Z_{O2}=...=Z_{On}$ and $R_{ST1}=R_{ST2}=...R_{STn}$

$$R_E \leq (7.10 * Z_O + R_{ST}) / n \qquad \text{(eqt. 32)}$$

where n is the number of parallel circuits.

For the 100E series

$$1 / R_E \geq 1 / (6.56*Z_{O1} - R_{ST1}) + 1 / (6.56*Z_{O2} - R_{ST2}) + 1 / (6.56*Z_{O3} - R_{STn})$$

For the case where $Z_{O1}=Z_{O2}=...=Z_{On}$ and $R_{ST1}=R_{ST2}=...R_{STn}$

$$R_E \leq (6.56 * Z_O + R_{ST}) / n \qquad \text{(eqt. 33)}$$

where n is the number of parallel circuits.

When a series terminated line is driving more than a single ECL load the issue of maximum number of loads must be addressed. The factor limiting the number of loads is the voltage drop across the termination resistor caused by the input currents to the ECL loads when the loads are in the quiescent high state. A good rule of thumb is to determine if the loss in high state noise margin is acceptable. The loss in noise margin is given by

$$NM_{LOSS} = I_T * (R_{ST} + R_O) \qquad \text{(eqt. 34)}$$

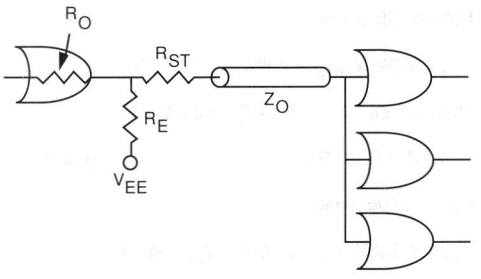


Figure 3.22 - Noise Margin Loss Example

where:
I_T = Sum of I_{INH} Currents

For the majority of devices in the ECLinPS family the typical maximum value for quiescent high state input current is 150µA. Thus for the circuit shown in Figure 3.22 in which three gate loads are present in a 50Ω environment the loss in high state noise margin is calculated as:

$NM_{LOSS} = 3 * 150\mu A * 50\Omega = 22.5mV$

ECLinPS I/O SPICE Modeling Kit

Due to the heavier reliance on simulation tools for initial prototyping, Motorola has put together a SPICE modeling kit aimed at aiding the customer in modeling board interconnect behavior. The kit includes representative drivers and receivers as well as the necessary SPICE model parameters. In addition tips are provided for simulating a wide range of output conditions. The kit, in conjunction with todays CAD tools, can greatly simplify the design and characterization of critical nets in a design. Anyone interested in obtaining a copy is encouraged to contact an ECLinPS Application Engineer.

SECTION 4
Interfacing with ECLinPS

Interfacing to Existing ECL Families

There currently exists two basic standards for high performance ECL logic devices: 10KH and 100K. To maximize system flexibility each member of the ECLinPS family is available in both of the existing ECL standards: 10E series devices are compatible with the MECL 10KH family; 100E series devices are compatible with ECL 100K.

The difference in the DC behavior of the outputs of the two different standards necessitates caution when mixing the two technologies into a single ended input design. As illustrated in Figure 4.1 and Table 4.1, there is no problem when a 10KH device is used to drive a 100K device, however problems arise when the scenario is reversed.

For the case of a 100K device driving a 10KH device the worst case noise margin is reduced to 35mV, a noise margin which is unacceptable for most designs. Since the problems of interfacing are an output tracking rate vs a V_{BB} tracking rate problem if the system uses only differential interconnect between the two technologies there will be no loss of noise margin and the design will operate as desired.

Fortunately the ECLinPS family, by offering devices in both standards, allows the user to integrate higher performance technology into his design without having to battle these interface problems.

Another area of concern when interfacing to older slower logic families is the behavior of ECLinPS devices with slower input edge rates. Typically, other than clock inputs, the ECLinPS family will function properly for edge speeds of up to 20ns. For edges significantly slower than 20nS the Schmitt trigger circuit of Figure 4.2 can be used to sharpen the edge rates reliably.

Obviously a very slow edge rate will amplify differences in delay paths due to any offset of the V_{BB} switching reference. This extra delay should be included in speed calculations of a design. For calculation purposes a worst case ±200ps/ns gate-gain delay (delay vs input edge rate) can be assumed or a more typical value of ±75ps/ns can be used.

Drvr > Rcvr	NM - High	NM - Low
10KH > 10KH	150mV	150mV
10KH > 100K	145mV	125mV
100K > 100K	130mV	135mV
100K > 10KH	35mV	130mV

Table 4.1 - Worst-Case Noise Margins of a Mixed 10KH and 100K Design

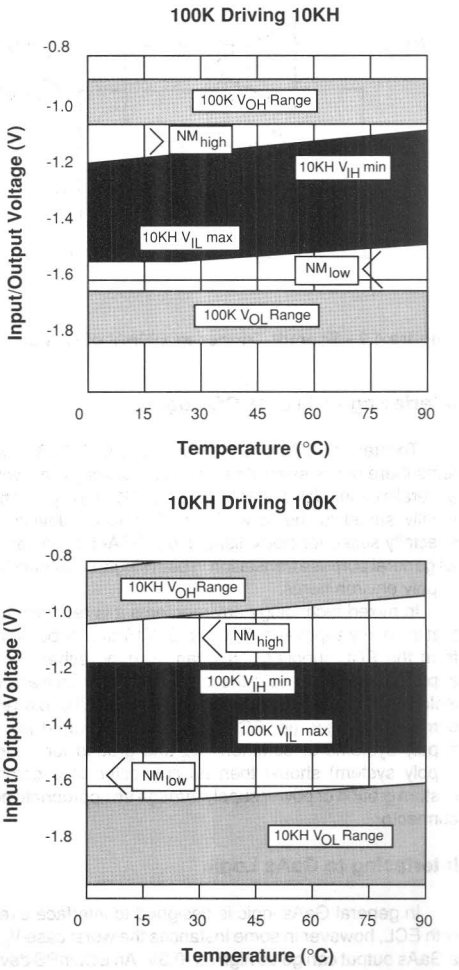


Figure 4.1 - Interfacing 10KH ECL and 100K ECL

Clock inputs on flip flop devices in the ECLinPS family are especially sensitive to slow edge rates. Flip flops have been successfully clocked in a noise free bench setup environment with edge rates of up to 20ns. However in ATE systems where more noise is present clocking problems arise with input edge rates of greater than 6 or 7ns. To ensure reliable operation in a system with input clock edges slower than 7ns it is recommended that the signals be buffered with an ECLinPS buffer circuit (E122, E116, E101 etc) or, for extreme conditions, the Schmitt trigger of Figure 4.2 to provide the gain necessary to sharpen the edges on the clock pulse.

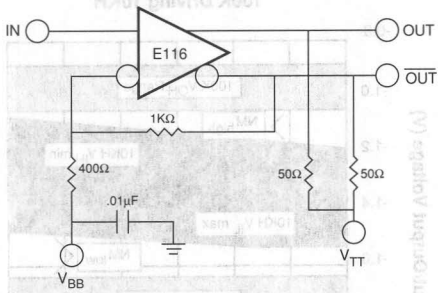


Figure 4.2 - Schmitt Trigger w/ 100mV of Hysteresis

Interfacing to TTL/CMOS Logic

To interface ECLinPS devices to TTL or CMOS subsystems there exists several new product offerings, as well as several existing devices, in the MECL 10KH family which are ideally suited to the task. These translation devices are specially suited for clock distribution, DRAM driving as well as general purpose translation in both single supply and dual supply environments.

In mixed technology environments it is recommended that the noisy supplies of TTL and CMOS circuits be isolated from the ECL supplies. This can be done either through separate power planes in the board or a common plane with isolated ECL and TTL power sub-planes. The planes of common voltages (ie. ECL V_{CC} and TTL ground for split supply systems or common V_{CC} and ground for a single supply system) should then be connected to a common system ground or power supply through an appropriate edge connector.

Interfacing to GaAs Logic

In general GaAs logic is designed to interface directly with ECL, however in some instances the worst case V_{OH} of a GaAs output can go as high as -0.3V. An ECLinPS device, depending on the input structure, may become saturated when driven with a -0.3V signal. It is recommended that if the designer is using a GaAs device which produces these -.3V signals in an ECLinPS design he contact a Motorola Applications Engineer to determine if the ECLinPS device being driven will be susceptible to saturation.

AC Coupling

In some cases it may be necessary to interface an ECLinPS design with a signal which lacks any DC offset. The differential devices in the ECLinPS family are ideally suited for this application. As pictured in Figure 4.3 the signal can be AC coupled and biased around the V_{BB} switching reference of the device. Note that this scheme only works for a data stream with no DC bias, for data streams such as RZ or unencoded NRZ DC restoration must be performed prior to AC coupling it to an ECLinPS device.

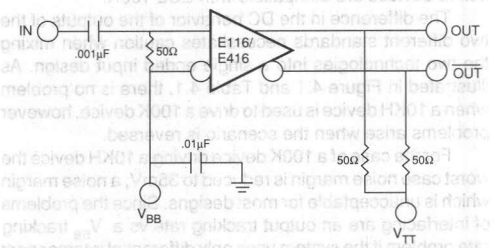


Figure 4.3 - AC Couple Circuit

The 50Ω resistor of Figure 4.3 provides the termination impedance while the V_{BB} pin provides the DC offset. The capacitor used to couple the signal must have an impedance of <<50Ω for all frequency components of the input signal. Because large capacitors appear somewhat inductive at high frequencies it may be necessary to use a small capacitor in parallel with a larger one to achieve satisfactory operation. In addition it is important to bypass the V_{BB} line when used in this manner to minimize the noise coupled into the device.

Because the AC signal is biased around V_{BB}, the output of the ECLinPS device when AC coupled will have a duty cycle identical to the input. Thus this type of application is ideal for transforming high frequency sinusoidal waveforms from an oscillator into a square wave with a 50% duty cycle. The E416 device is a specialized line receiver with a much higher bandwidth than alternative ECLinPS devices, therefore for frequencies of >500MHz it is recommended that the designer use this device.

The above mentioned scenario will work fine as long as the input signal is present, however if the the inputs to the AC coupled device are left open problems may occur. With no input signal both inputs will go to V_{BB} and an undefined output, and perhaps an oscillating output, will result. If a defined output is necessary for an open input scenario, the

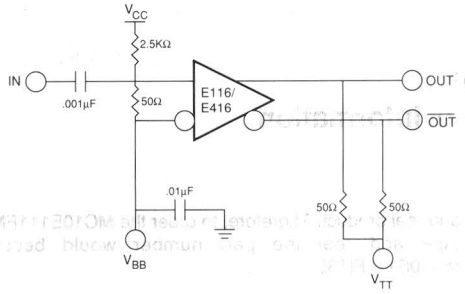


Figure 4.4 - AC Couple Circuit with DC Offset

circuit of Figure 4.4 can be used. The resistor tree between V_{CC} and V_{BB} creates an offset between the two inputs so that if the driving signal is lost a stable defined output will occur.

Unfortunately this configuration will adversely affect the duty cycle of the output. Depending on the frequency of the output, the duty cycle will change due to the longer distance to threshold on a rising edge as opposed to a falling edge. With this in mind it becomes obvious that the smallest feasible offset would be the best solution. For stability a minimum of 25mV is recommended, however this will not produce full ECL levels at the outputs of an E116 and thus another differential gate should be used to further amplify the signal. The gain of the E416 on the other hand is sufficient to produce acceptable levels at the outputs for DC input voltage differences of 25mV. If a 150mV offset is used full ECL levels will be seen at the outputs of the E116 however the price in duty cycle skew will be high. Of course if the signal is divided after it is received the duty cycle will be restored.

When using the circuit of Figure 4.4 care should be taken to limit the current sunk by the V_{BB} pin to a maximum of 0.5mA. To achieve an offset of greater than 25mV for the circuit of Figure 4.4 the DC current will necessarily need to be greater than 0.5mA. To alleviate this dillema one of the gates of the E116 can be configured as pictured in Figure 4.5 to generate a V_{BB} reference with the necessary current sinking capability. A single gate configured in this way will source or sink up to 10mA without a significant shift in the generated V_{BB} level. If more current is needed several gates can be connected in parallel to provide the extra drive capability.

Note that the circuit pictured in Figure 4.4 will result in the Q outputs going high when the inputs are left open. If the opposite is desired the resistor to V_{CC} can be tied to the inverting input and V_{BB} to the non-inverting input.

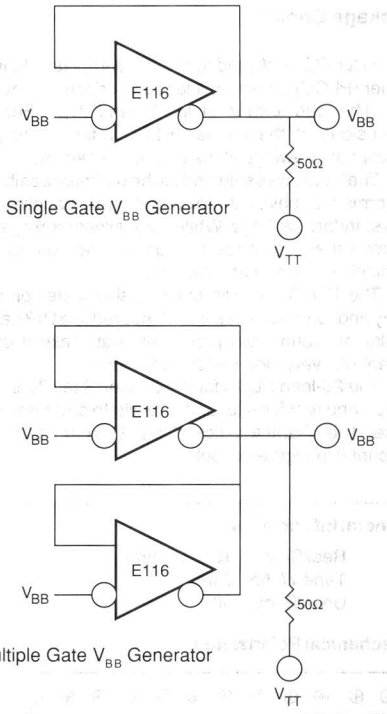


Figure 4.5 - High Current V_{BB} Generator

carrier (PLCC) package, a leaded surface mount IC package. The lead form is of the "J-lead" type. For detailed dimensions of the 28-lead PLCC refer to the package description drawings at the end of this section.

The PLCC was selected as the optimum combination of performance, physical size and thermal handling in a low cost standard package. While more exotic packages exist to improve these qualities still further, the cost of these is prohibitive for many applications.

The PLCC features considerably faster propagation delay and reduced parasitics compared to a DIP package of similar pin-count; two properties that make it eminently suitable for very high performance logic.

The 28-lead PLCC for the ECLinPS family is available in tape and reel form to further facilitate automatic pick and place. The characteristics of the 28-lead PLCC reel are described in Figure 5.1 below.

General Information

Reel Size: 13" (330mm)
Tape Width: 24mm
Units/Reel: 500

Mechanical Polarization

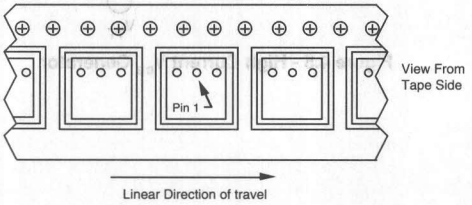


Figure 5.1 - 28-Lead PLCC Tape & Reel Information

To order ECLinPS in tape and reel form a minimum 3000 piece order per device type is required. In addition orders must be full reels or multiples of full reels as no partial reels will be shipped. An R2 suffix has been established to add to the end of the part number to signify the desire for tape

Reliability of Plastic Packages

Although today's plastic packages are as reliable as ceramic packages under most environmental conditions, as the junction temperature increases a failure mode unique to plastic packages becomes a significant factor in the long term reliability of the device.

Modern plastic package assembly utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. As the temperature of the silicon (junction temperature) increases an intermetallic compound forms between the gold and aluminum interface. This intermetallic formation results in a significant increase in the impedance of the wire bond and can lead to performance failure of the affected pin. With this relationship between intermetallic formation and junction temperature established it is incumbent on the designer to ensure that the junction temperature for which a device will operate is consistent with the long term reliability goals of the system.

Reliability studies were performed at elevated ambient temperatures (125°C) from which an arrhenius equation relating junction temperature to bond failure was established. The application of this equation yields the table of Figure 5.2. This table relates the junction temperature of a device in a plastic package to the continuous operating time before 0.1% bond failure (1 failure per 1000 bonds)

ECLinPS devices are designed with chip power levels that permit acceptable reliability levels, in most systems, under the conventional 500lfpm (2.5m/s) airflow.

Thermal Management

As in any system, proper thermal management is essential to establish the appropriate trade-off between performance, density, reliability and cost. In particular, the designer should be aware of the reliability implication of continuously operating semiconductor devices at high junction temperatures.

The increasing popularity of surface mount devices (SMD) is putting a greater emphasis on the need for better thermal management of a system. This is due to the fact that SMD packages generally require less board space than their through hole counterparts so that designs incorporating

$$T = 6.376 \times 10^{-9}\, e^{\left[\frac{11554.267}{273.15 + T_J}\right]}$$

Where:
T = Time to .1% bond failure

Junction Temp. (°C)	Time (Hrs.)	Time (Yrs.)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.1
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Figure 5.2 - T_J vs Time to .1% Bond Failure

SMD technologies have a higher thermal density. To optimize the thermal management of a system it is imperative that the user understand all of the variables which contribute to the junction temperature of the device.

The variables involved in determining the junction temperature of a device are both supplier and user defined. The supplier through lead frame design, mold compounds, die size and die attach can positively impact the thermal resistance and thus the junction temperature of a device. Motorola continually experiments with new package designs and assembly techniques in an attempt to further enhance the thermal performance of its products.

It can be argued that the user has the greatest control of the variables which commonly impact the thermal performance of a device. Ambient temperature, air flow and related cooling techniques are the obvious user controlled variables, however PCB substrate material, layout density, size of the air-gap between the board and the package, amount of exposed copper interconnect, use of thermally-conductive epoxies and number of boards in a box can all have significant impacts on the thermal performance of a system.

PCB substrates all have different thermal characteristics, these characteristics should be considered when exploring the PCB alternatives. The user should also account for the different power dissipations of the different devices in his system and space them on the PCB accordingly. In this way the heat load is spread across a larger area and "hot spots" do not appear in the layout. Copper interconnect traces act as heat radiators therefore significant thermal dissipation can be achieved through the addition of interconnect traces on the top layer of the board. Finally the use of thermally conductive epoxies can accelerate the transfer of heat from the device to the PCB where it can more easily be passed to the ambient.

The advent of SMD packaging and the industry push towards smaller denser designs makes it incumbent on the designer to provide for the removal of thermal energy from the system. Users should be aware that they control many of the variables which impact the junction temperatures and thus to some extent the long term reliability of their designs.

Calculating Junction Temperature

The following equation can be used to estimate the junction temperature of a device in a given environment:

$T_J = T_A + P_D\Theta_{JA}$ where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
Θ_{JA} = Avg Pkg Thermal Resistance (Junction - Ambient)

The power dissipation factor is made up of two elements: the internal gate power and the power associated with the output terminations. Essentially the two contributors can be calculated separately, then added to give the total power dissipation for a device.

To calculate the power of the internal gates the user simply multiplies the I_{EE} of the device times V_{EE}. Since I_{EE} in ECL is a constant parameter frequency need not be factored into the calculations. A worst case or typical number for chip power can be calculated by using either worst case or typical data book values for the I_{EE} and V_{EE} of a device.

Next the power of the outputs needs to calculated so that the total power dissipation for a device can be determined. The output power is dependent on the termination resistance and the termination scheme used to pulldown the outputs. The most typical termination scheme for ECLinPS designs is a parallel termination into -2.0V. For this scheme the following equation describes the power for a single output of the device:

$P_{Dout} = I_{OUT} * V_{OUT} = (V_{OUT} - (-2))/R_T * V_{OUT}$ where:

V_{OUT} = V_{OH} or V_{OL}
R_T = Termination Resistance

The power dissipated in the output of a device is dependent on the duty cycle of that output. For an output terminated to V_{TT} the worst case situation would be if the output was in the high state all of the time, for an output terminated to V_{EE} the low state will represent worst case. For single ended output devices typically the power is calculated with the outputs in the worst case and for a 50% duty cycle. For differential outputs the power for a differential pair is constant since they are always in complimentary states, therefore for a given output the power will simply be the average of the high and low state output powers. Figure 5.3 shows the various output power levels for the different output types and conditions. In addition the table includes power numbers for various other

Termination Resistance	Output Power (mW)					
	Differential Output		Single-ended Output (50% Duty Cycle)		Single-ended Output (Worst Case)	
	10E	100E	10E	100E	10E	100E
50 to -2.0V	14.3	15.0	14.3	15.0	19.8	20.0
68 to -2.0V	10.5	11.1	10.5	11.1	14.6	14.7
100 to -2.0V	7.1	7.5	7.1	7.5	9.9	10.0
510 to -5.2V	9.7	9.8	9.7	9.8	11.8	11.7
330 to -5.2V	15.0	15.1	15.0	15.1	18.3	18.0
180 to -5.2V	27.5	27.8	27.5	27.8	33.5	33.1
510 to -4.5V	-	7.8	-	7.8	-	9.3
330 to -4.5V	-	12.3	-	12.3		14.4
180 to -4.5V	-	22.6	-	22.6	-	26.4

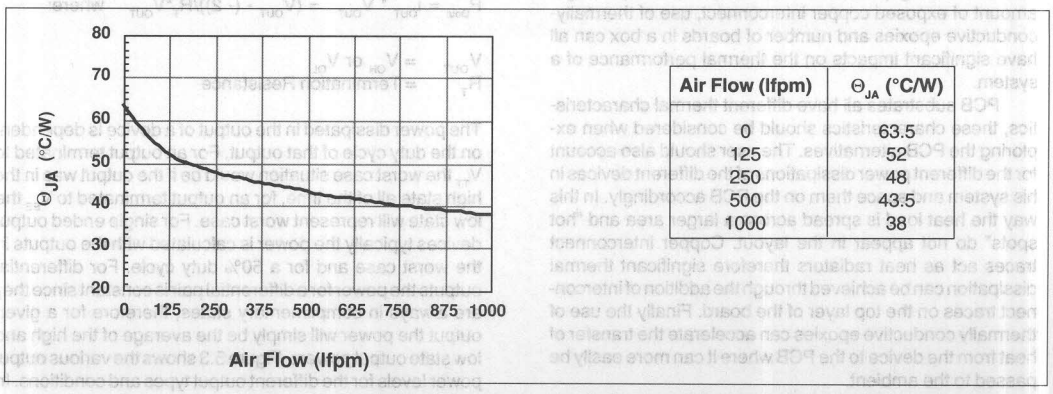
Figure 5.3 - Output Power for Various Termination Schemes

termination resistances and alternative termination schemes. These numbers can be derived by determining the I_{OUT} and V_{OUT} for the different alternatives and applying the equation above.

Now that the power dissipation of a device can be calculated one needs to determine which level of the parameter (ie. typical, max etc..) to use to estimate the long term reliability of the system. Since this number is statistical in nature simply applying the worst case numbers will be overly pessimistic as these parameters vary statistically themselves. It is not very likely, for instance, that every device type will be operating at the maximum specified I_{EE} level. Assuming all worst case conditions can have a significant impact on the resulting junction temperature estimates leading to erroneous conclusions about the reliability of the design.

Another important parameter for calculating the junction temperature of a device is the junction-ambient thermal resistance, Θ_{JA}, of the package. Θ_{JA} is expressed in °C per watt (°C/W) and is used to determine the temperature elevation of the die (junction) over the external package ambient temperature. Standard lab measurements of this parameter for the 28-lead PLCC yields the graph of figure 5.4.

An alternative calculation scheme for T_J substitutes the case temperature (T_C) and the junction-to-case (Θ_{JC}) thermal resistance for their ambient counterparts in the T_J equation previously mentioned. The Θ_{JC} for the 28-lead PLCC is 32°C/W. This parameter is measured by submerging the device in a liquid bath and measuring the temperature of the bath, therefore it represents an average case temperature. The difficulty in using this method arises in the determination



Air Flow (lfpm)	Θ_{JA} (°C/W)
0	63.5
125	52
250	48
500	43.5
1000	38

Figure 5.4 - Thermal Resistance vs Air Flow for the 28-lead PLCC

of the case temperature in an actual system. The case temperature is a function of the location at which the temperature is measured on the package. Therefore to use the Θ_{JC} mentioned above the case temperature would have to be measured at several different points and averaged to represent the T_C of the device. This in practice could prove difficult and relatively inaccurate.

Junction Temperature Calculation Example

As an example the power dissipation for a 10E151 6-bit register function will be calculated for 500 lfpm airflow; both a worst case number and a typical number will be calculated. From the data sheet the typical and maximum I_{EE}'s for the device are 65mA and 85mA respectively. There are six differential output pairs.

Chip Power =
65mA * 5.2V = 338mW typical
85mA * 5.46V = 464mW worst case

Output Power =
((-1.75 - (-2))/50*1.75 + (-.9 - (-2))/50*.9))/2 = 14.3mW

Total Power Pd =
338mW + 14.3*12 = 510mW typical
464mW + 14.3*12 = 635mW worst case

Junction Temperature =
T_A + 43.5°C/W*.510W = T_A + 22°C typical
T_A + 43.5°C/W*.635W = T_A + 28°C worst case

Note that in this case the worst case junction temperatures are not significantly larger than the typical case. This is due mainly to the fact that the device has differential outputs. A higher I_{EE}, single ended device would show a much larger discrepancy between the worst case and typical values.

Limitations to Calculation Technique

The use of the previously described technique for estimating junction temperatures is intimately tied to the measured values of the Θ_{JA} of the 28-lead PLCC package. Since this parameter is a function of not only the package, but also the test fixture the results may not be applicable for every environmental condition. The 28-lead PLCC test fixture used was a 2.24" x 2.24" x .062" FR4 type glass epoxy board with 1oz. copper used for interconnects. The copper represented about 50% coverage of the test fixture.

If the users actual application does not come close to approximating this situation it may be necessary to use a different method for determining the junction temperature of a device. An empirical equation relating junction temperature to the actual case temperature and lead temperature of a device has been established. This equation has the advantage of being universal for all environmental conditions, however the disadvantage of having to make actual thermocouple temperature measurements may limit its use.

The equation describing the junction temperature is as follows:

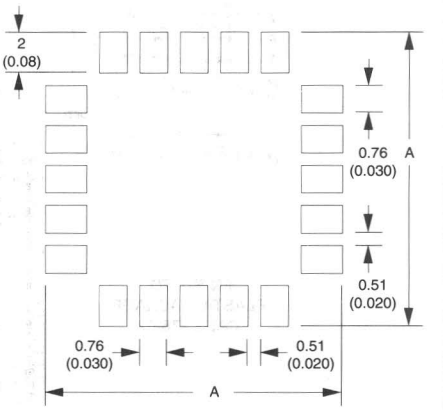
$T_J = 24P_D + .313T_C + .687T_L$ °C/W (±2°C/W)

where:
P_D = Power Dissipation of the Device (W)
T_C = Case Temperature (°C)
T_L = Lead Temperature (°C)

T_C is measured at the top-center surface of the package taking care that the thermocouple makes good contact with the case without transporting a significant amount of heat from the measurement point. The lead temperature is used to compensate for the differences in the ratio of heat transfer through the leads and the top surface of the package. This difference impacts the actual T_C of the package. As mentioned earlier this method of determining the junction temperature is effective for almost all environmental conditions except those that incorporate an external heat sink. Of all the techniques mentioned in this document, the application of this equation will lead to the most accurate assessment of the junction temperature of a device .

Heatsinks

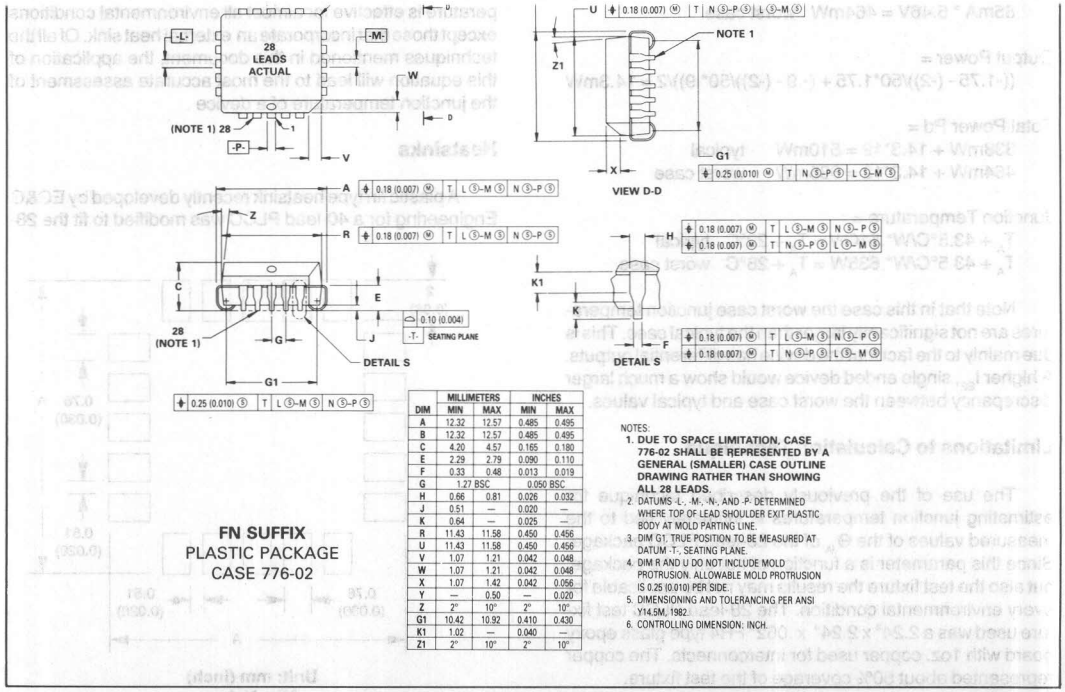
A plastic fin type heatsink recently developed by EG&G Engineering for a 40-lead PLCC was modified to fit the 28-



Unit: mm (inch)
Min. Value

Dimension A	Inches	mm
PLCC-20	0.430	10.9
PLCC-28	0.530	13.5
PLCC-44	0.630	16

Figure 5.5 - PLCC PCB Solder Pad Dimensions



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

Figure 5.6 — 28-Lead PLCC Dimensions

SECTION 6
Quality & Reliability

Quality

The Motorola culture is a culture of quality. Throughout all phases of product development, from defining and designing to shipping the product Motorola strives for total customer satisfaction through "Six Sigma" and "On Time Delivery" programs.

Defining Products

From the beginning the goal of the ECLinPS family was to be "customer" defined. Extensive work was done up front to identify part types which were perfectly suited to the needs of our customers. This definition phase ensured a level of quality for the family in that the customer defines the product rather than the supplier dictating product types.

Designing Products

Superior quality products start with the design, and the design of a product starts with an IC process. Extensive work was done with the MOSAIC III process to ensure a solid platform for quality products. Process reliability studies were performed to uncover any weaknesses in the initial process so that enhancements could be made to strengthen it before it was released to production. In addition comprehensive characterization and correlation work was completed on the process to ensure the utmost in modeling parameter accuracy.

The design of the products strictly adhered to the design rules set forth by the process designers. Conservative, manufacturable layout rules were followed to minimize the performance variability due to a marginally manufacturable product. In addition the use of statistical modeling methods, such as factorial and response surface techniques, in the designing of the IC's leads to products with a reduced sensitivity to variations in the manufacturing process.

Manufacturing Process

Through SPC and continual engineering work, the manufacture of the MOSAIC III process is both monitored and enhanced on a continuous basis. Statistical data is gathered at both probe and final test through nth device data collection to monitor the distribution of a parameter to its specification limits. In addition final quality assurance gates are set up to guarantee the quality of outgoing product.

Product Characterization

Products are both DC and AC characterized for all data book environmental conditions prior to the release of the product to production. The distributions of the parameters are compared to their specification limits to ensure that Motorola "manufactures" quality products as opposed to "testing" quality products through distribution truncation. In addition ongoing AC characterization is performed to enhance the distributions of the AC parameters of the device. In doing so as the distributions warrant, further enhancements to the AC specifications can be achieved.

Reliability

To ensure the long term reliability of ECLinPS products extensive accelerated life testing is performed prior to production release. This qualification work is performed by Logic Reliability Engineering, an organization specifically dedicated to monitoring and guaranteeing the quality and and reliability of logic products. The accelerated life test consists of the following:

Operating Life Test - 145°C Mil. Std. 883
Temperature Cycle - -65°C to 150°C Mil. Std. 883
Pressure, Temperature, Humidity (Hermeticity)

A minimum of two lots, 250 die per lot taken from three different wafers in the lot constitute a qualification sample. Various intermediate readouts are taken to monitor the performance more closely. In addition the devices are tested beyond the specification limits to determine where and how they will fail.

Another responsibility of the reliability group is that of failure analysis. This failure analysis service is supported for both internal purposes and for servicing the needs of our customers. Analysis entails everything from simple package examination to internal microprobing to SEM analysis of IC structures. The results of the analysis are returned to the customer and if the analysis suggests a potential problem with the device the information is also passed to the internal product groups.

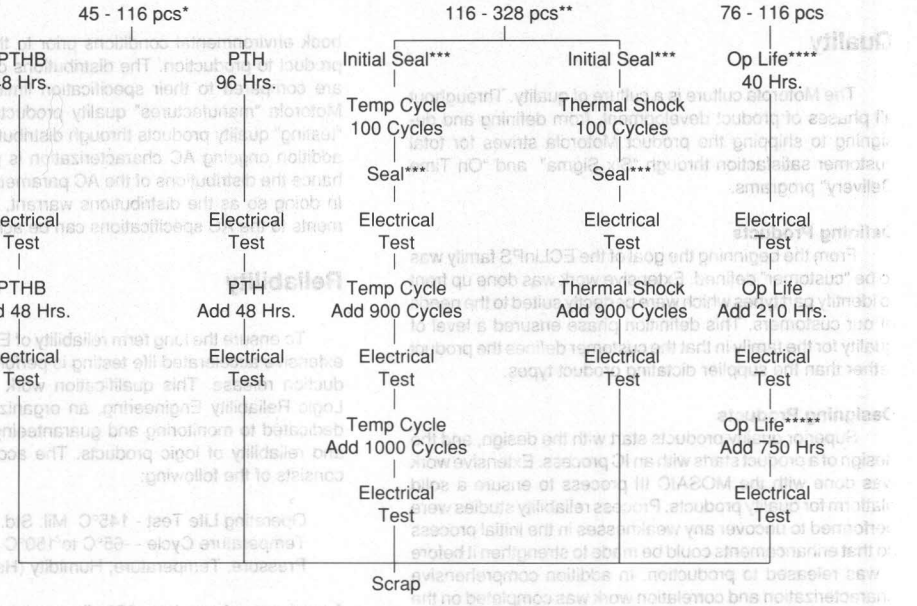
RAP: Reliability Audit Program

The Reliability Audit Program (RAP) developed in March 1977 is the Motorola internal reliability audit which is designed to assess outgoing product performance under accelerated stress conditions. Logic Reliability Engineering

has overall responsibility for RAP, including updating its requirements, interpreting its results, administration at off-shore locations and monthly reporting of results. These reports are available at all sales offices. Also available is the "Reliability and Quality Handbook" which contains data for all Motorola semiconductors (#BR518S).

Rap is a system of environmental and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives the tests specified in Figure 6.1. Frequency of testing is specified per internal document 12MRM15301A.

Figure 6.1 - Reliability Audit Program Test Flow



* PTH will be run as a substitute if PTHB sockets are not available. Only required on plastics packages.

** Thermal Shock will be run if Temp Cycle is not available.

*** Seal (fine and gross) only required on hermetic packages.

**** All units for Op Life to be AC/DC tested before and after being stressed. All units failing AC after stress will be analyzed.

***** One sample per month

PTHB
15psig/121°C/100% RH at rated V_{CC} or V_{EE} - to be performed on plastic encapsulated devices only.

Temp Cycle
Mil. Std. 883, Method 1010, Condition C, -65°C to 150°C

Op Life
Mil. Std. 883, Method 1005, Condition C (Power plus Reverse Bias), T_A = 145°C.

Notes:
1. All standard 25°C DC and functional parameters will be measured Go/NoGo at each readout.
2. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.
3. Sampling to include all package types routinely.
4. Device types sampled will be by generic type within each digital IC product family (MECL, TTL, etc.) and will include all assembly locations (Korea, Phillipines, Malaysia, etc.).
5. 16 hrs. PTHB is equivalent to ≈800 hrs. of 85°C/85% RH THB for VCC ≤ 15V.
6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
7. Special device specifications (48A's) for digital products will reference 12MRM15301A as a source of generic data for any customer required monthly audit reports.